Welcome to the 12th
International Conference on
Nitride Semiconductors
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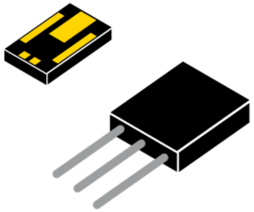
## C4.5

# Low vertical leakage current of 0.07 µm/mm$^2$ at 600 V without intentional doping for 7 µm-thick GaN-on-Si

**ALLOS Semiconductors GmbH**
**Atsushi Nishikawa**

# ALLOS' GaN-on-Si epi-technology is available for all major market segments

### HPE



**GaN-on-Si enables more efficient high power electronic (HPE) devices out of silicon lines**

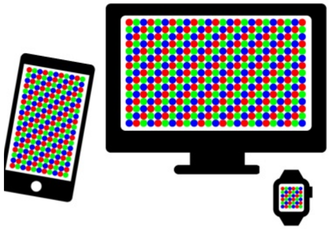
### RF

**GaN-on-Si provides higher performance and lower cost for RF devices**

### LED

**GaN-on-Si is a niche today but very high cost saving potential remains attractive for the future**

### Micro LED



**Only GaN-on-Si can deliver the super-uniform, CMOS-compatible large epi-wafers needed for micro LEDs**

**AlGaN/GaN HEMT on Si for high power electronics application**
is the main focus on this presentation

# Common believes about GaN-on-Si power electronics

*“You need carbon doping to achieve the required leakage current”*

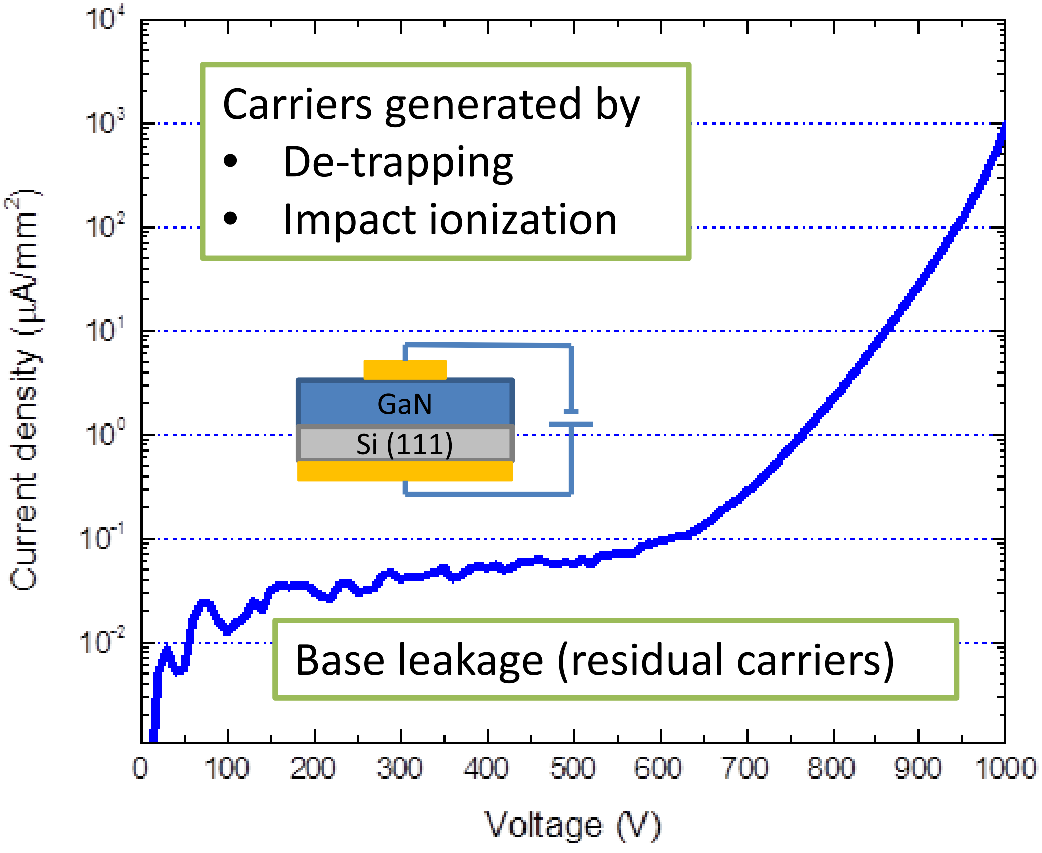
*“Interlayers are bad for leakage current control”*

*“The choice of the right reactor is decisive for the material and electrical properties you can achieve”*

# How to suppress the vertical leakage current?

## Causes for leakage

Typical I-V curve for vertical leakage measurement



Carriers generated by

- De-trapping
- Impact ionization

Base leakage (residual carriers)

## Typical measures to suppress leakage

| Measure | Mainstream approach | ALLOS' approach |
|---|---|---|
| Crystal quality improvement (Ec) | Usually not sufficient | **Very good results** |
| GaN thickness increases | Often causes cracks, bow, breakage | **Very good results** |
| Layer stack design | Individual technology tactics | **Very good results** |
| Trap carriers (e. g. C-doping) | **Works, but what about side-effects?** | Not used in this work |

| Common believes | Shown in this presentation |
|---|---|
| ~~*“You need carbon doping”*~~ | No – you can have very high isolation based on high-crystal quality and thick GaN. |
| ~~*“Interlayers are bad for leakage”*~~ | The opposite is true: Intelligently designed interlayers suppress the carrier multiplication process in the structure |

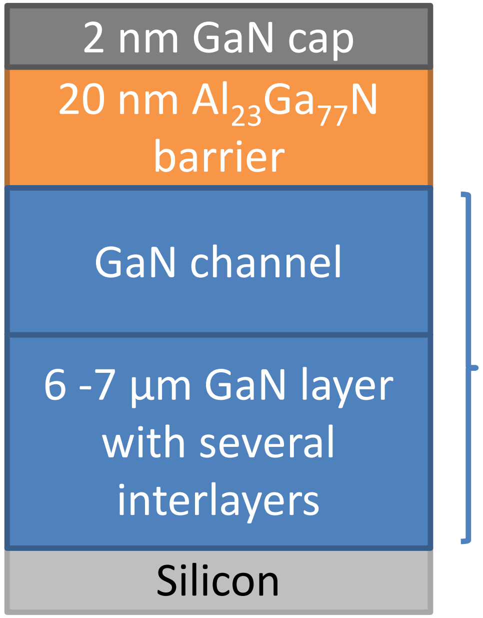
# MOCVD growth method and structure for this work

- Industry standard multi-wafer MOCVD reactors were used (Veeco K465i, AIXTRON G5)

- Substrate:  150 mm p-type Si (111)

- Impurity concentration in GaN measured by SIMS:
  - C:  ~ $7 \times 10^{16}$ cm$^{-3}$
  - O: ~ $7 \times 10^{16}$ cm$^{-3}$
  - H: < $1 \times 10^{18}$ cm$^{-3}$ (below detection limit)

HEMT structure



2 nm GaN cap

20 nm $Al_{23}Ga_{77}N$ barrier

GaN channel

6 -7 µm GaN layer with several interlayers

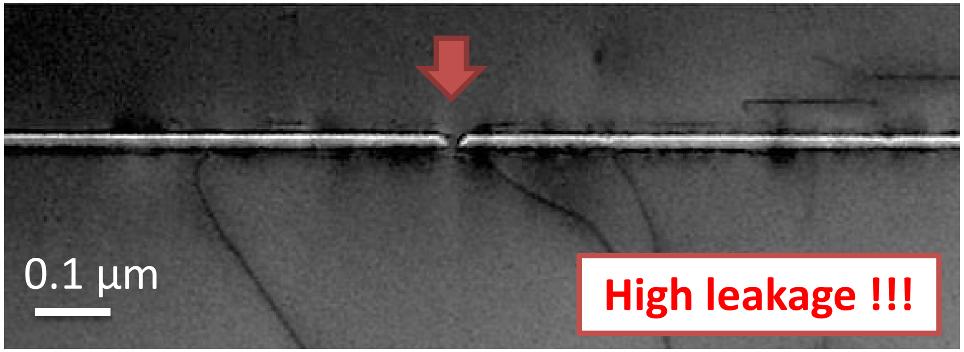
Silicon

Optimization parameters:

1. Crystal quality
2. GaN thickness
3. Interlayer position and amount

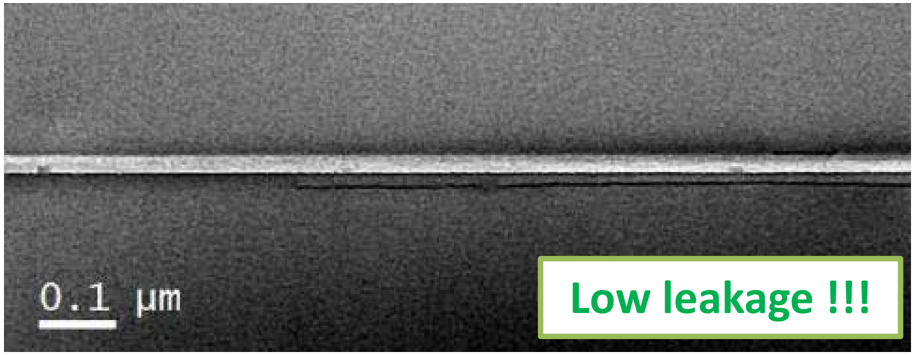
# Interlayer growth control is key feature for low leakage

**For example pit in interlayer (not good)**



**High leakage !!!**

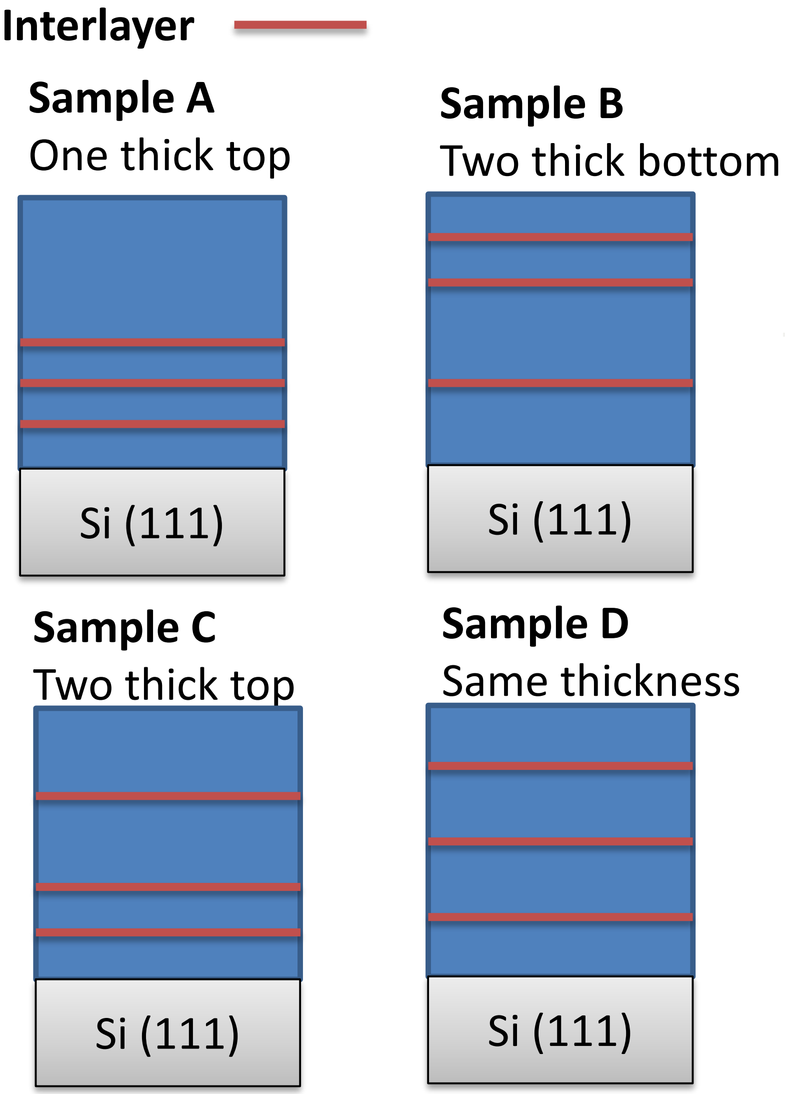
**High quality interlayer (good)**



**Low leakage !!!**

**Important how to design and grow interlayer**

# Optimized interlayer position reduces the vertical leakage current @ 600 V by one order of magnitude



**Interlayer**

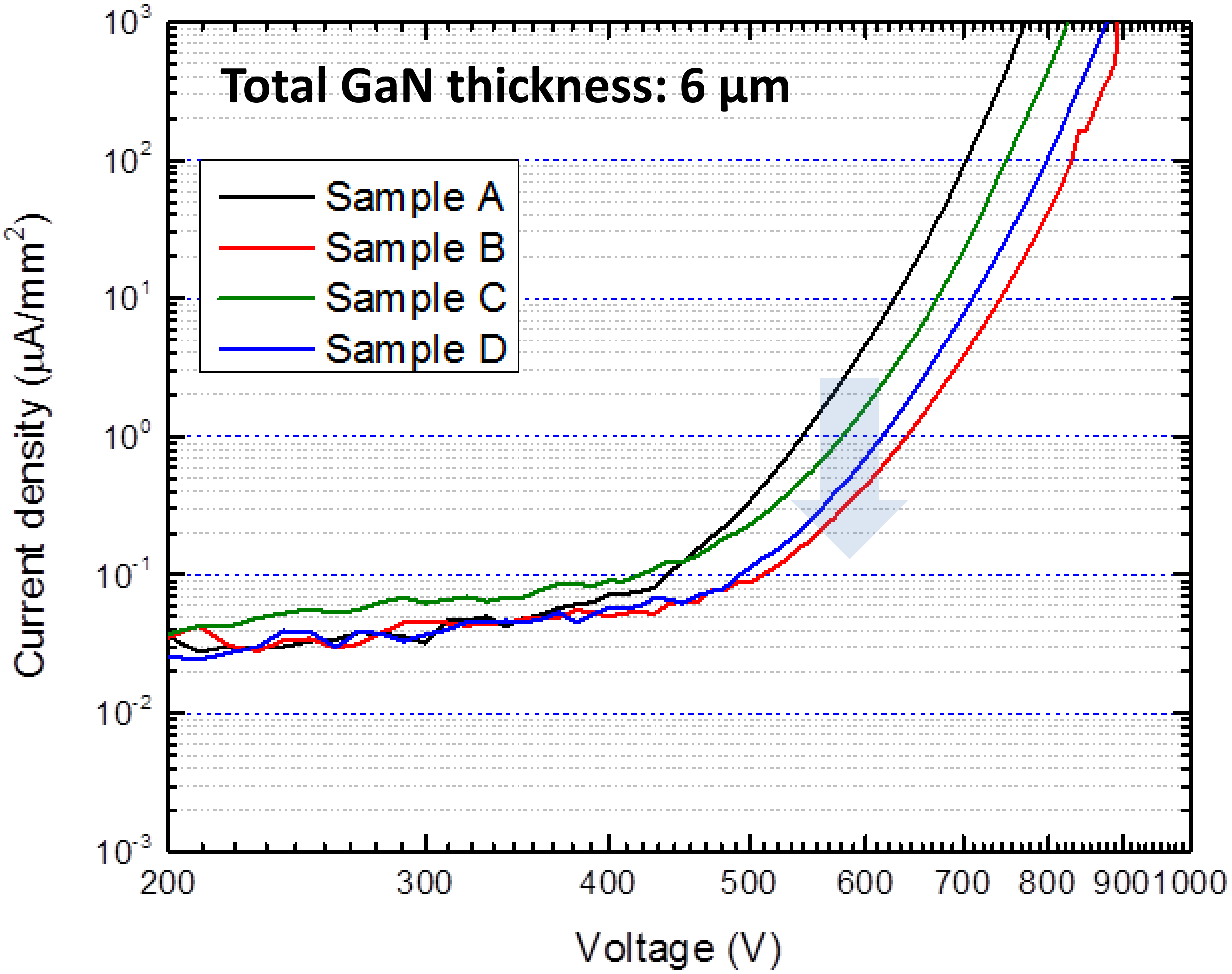
**Sample A**
One thick top

**Sample B**
Two thick bottom

**Sample C**
Two thick top

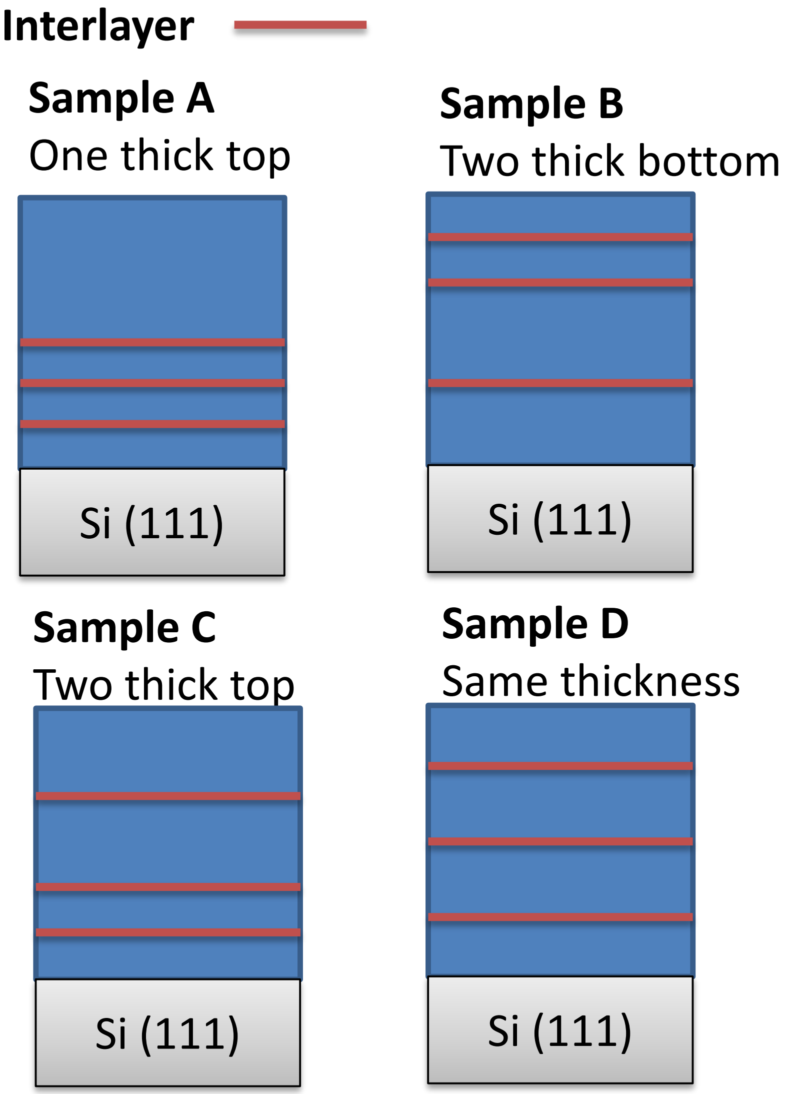
**Sample D**
Same thickness

**I-V curves for vertical leakage measurement in log-log plot**



**Total GaN thickness: 6 µm**

# Optimized interlayer position reduces the vertical leakage current @ 600 V by one order of magnitude



**Interlayer**

**Sample A**
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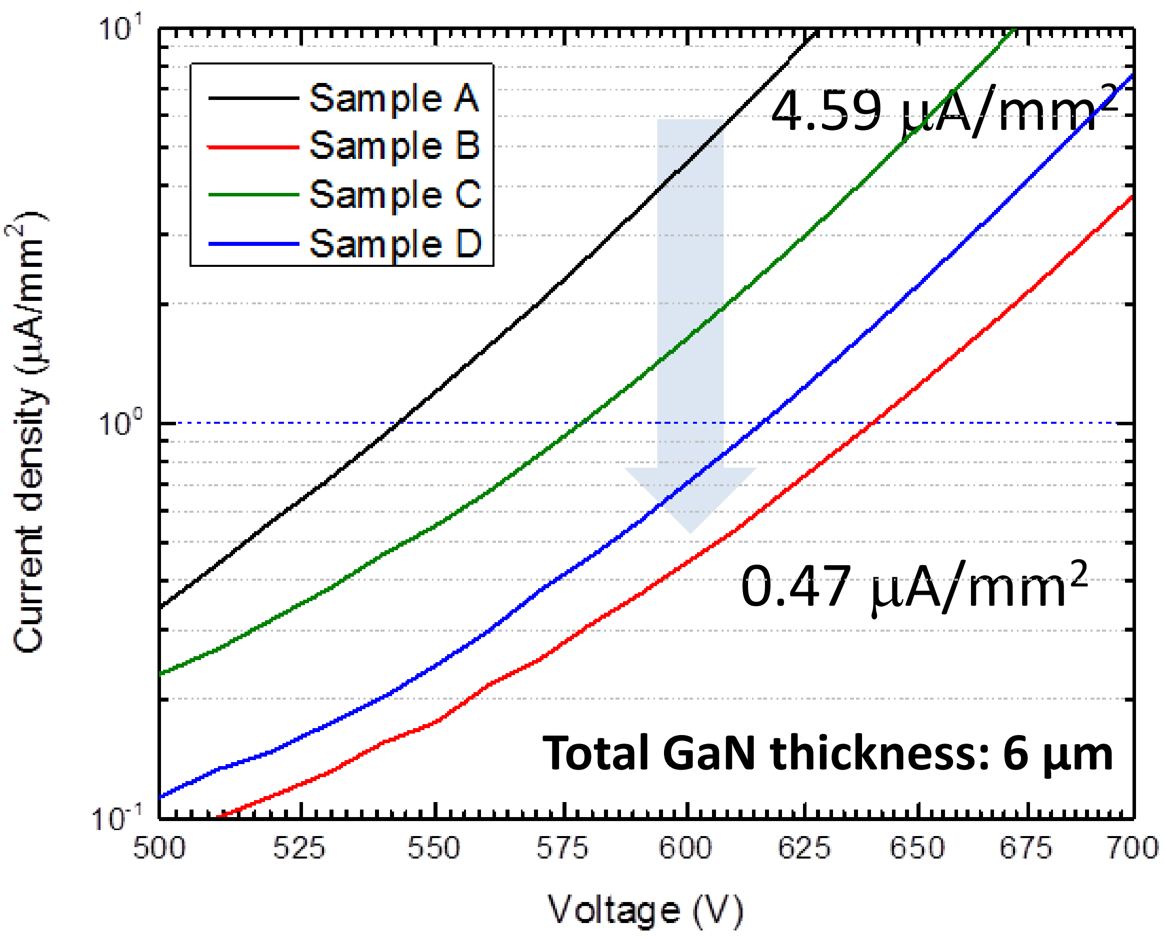
Same thickness

**I-V curves for vertical leakage measurement in log-log plot**

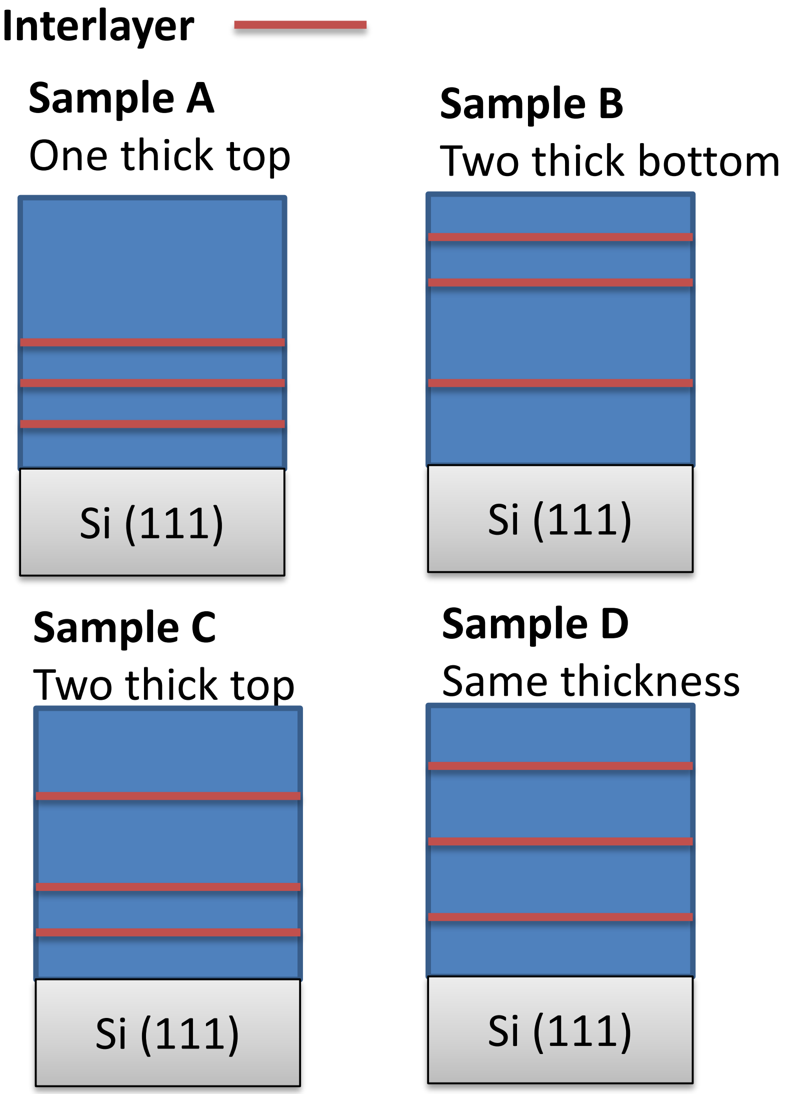


4.59 µA/mm²

0.47 µA/mm²

**Total GaN thickness: 6 µm**

# Leakage reduction is not caused by crystal quality which is similar for all interlayer positions



**Interlayer**

**Sample A**
One thick top

**Sample B**
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**Sample C**
Two thick top

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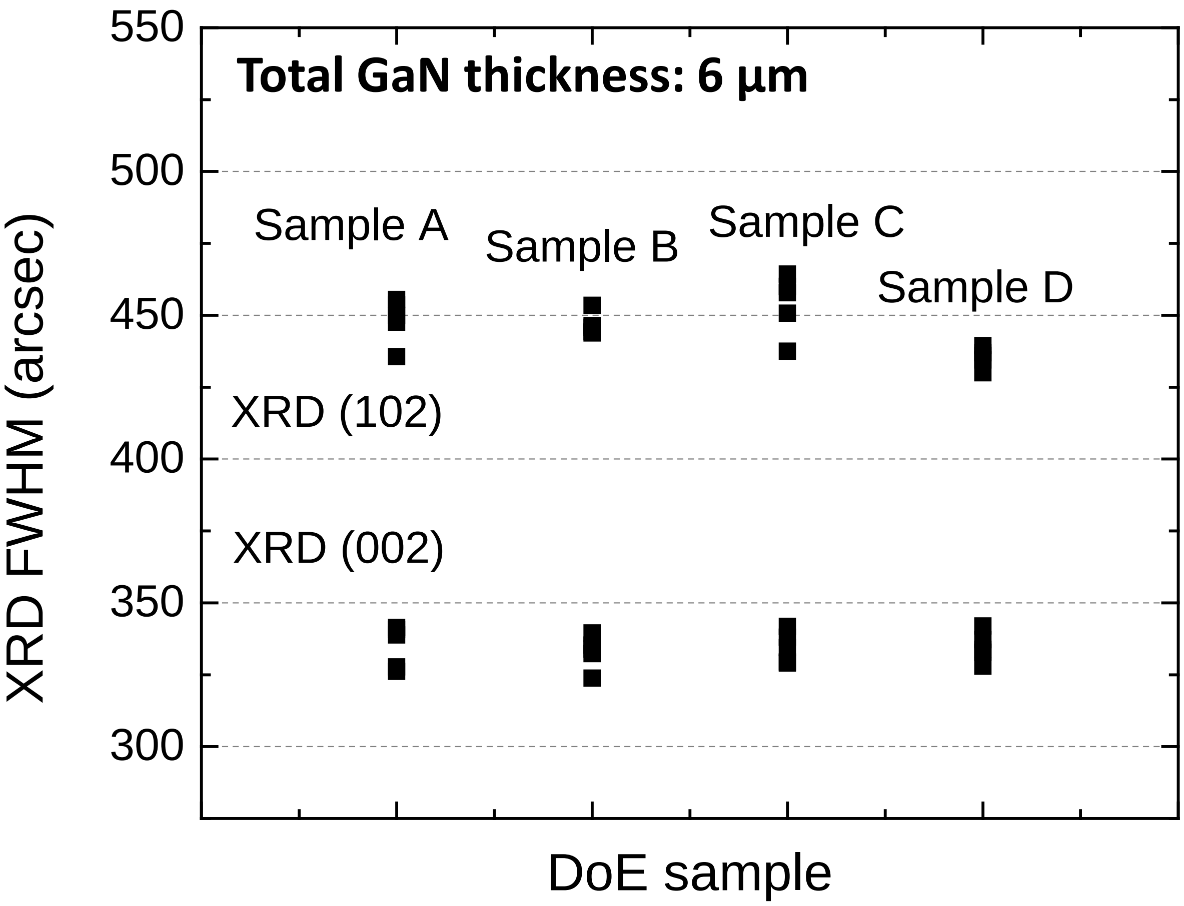
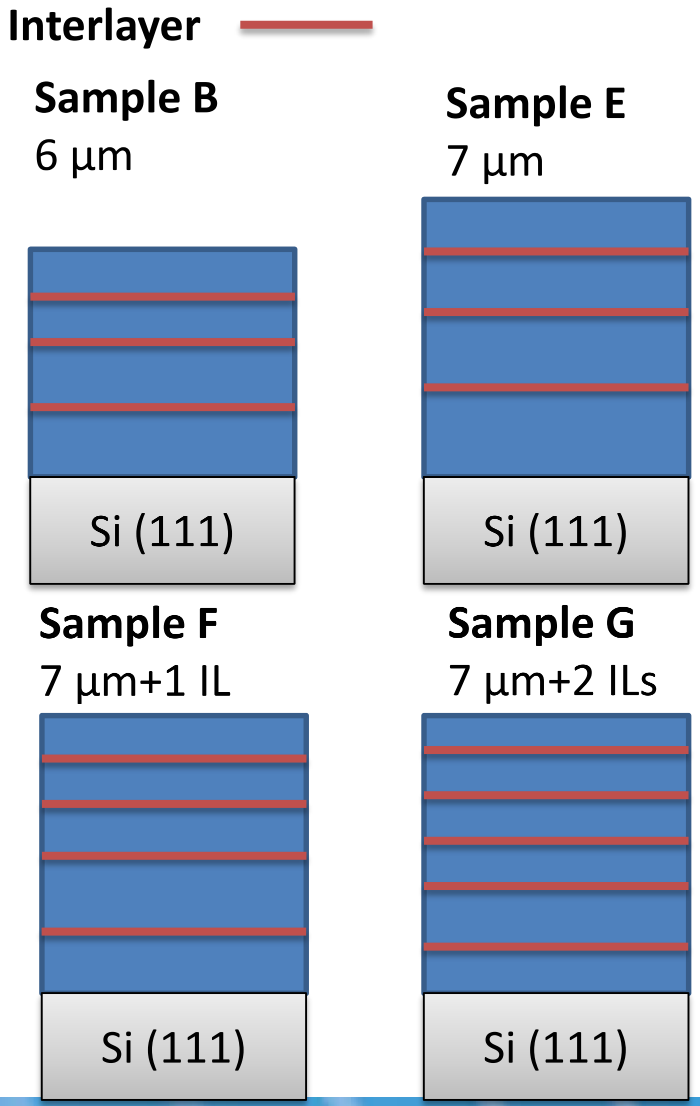
Same thickness



**Total GaN thickness: 6 µm**

# Further crystal quality improvement is achieved by further increasing GaN thickness from 6 to 7 µm



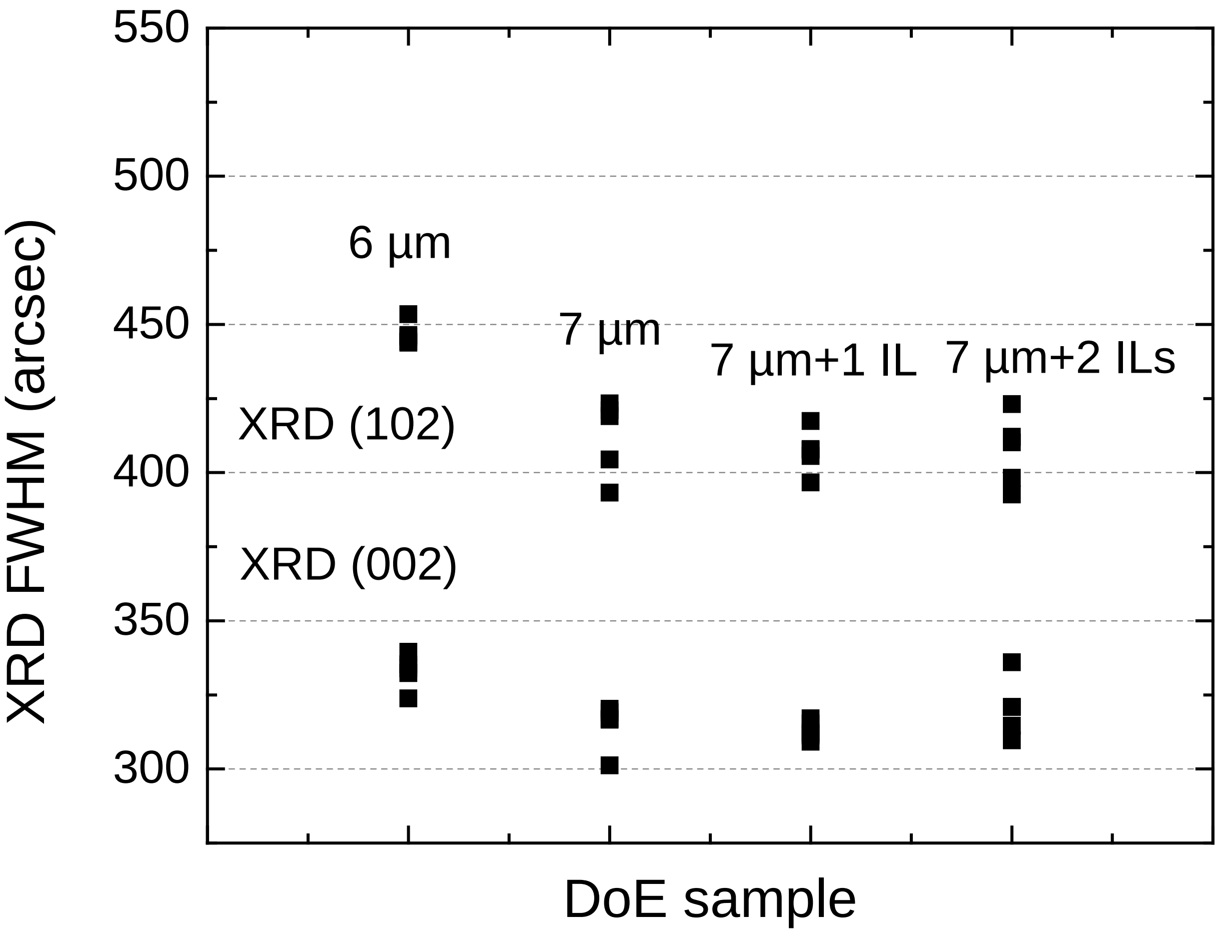
**Interlayer** —

**Sample B**
6 µm
Si (111)

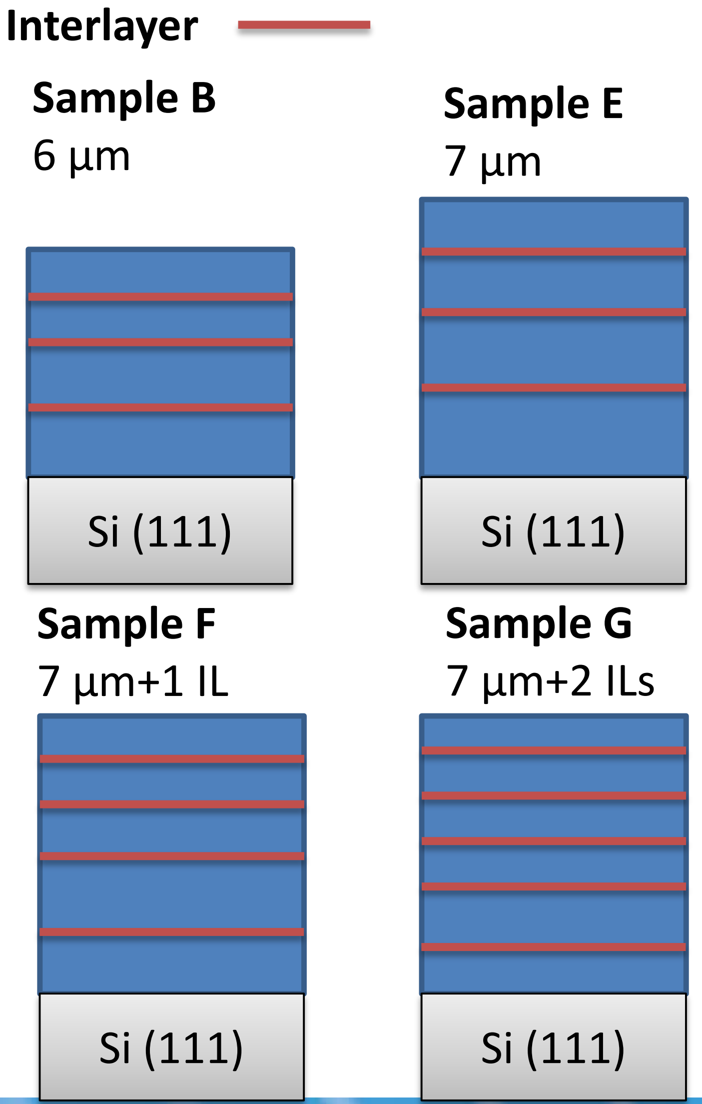
**Sample E**
7 µm
Si (111)

**Sample F**
7 µm+1 IL
Si (111)

**Sample G**
7 µm+2 ILs
Si (111)



# Thicker GaN layer with higher quality and additional interlayers suppress vertical leakage further



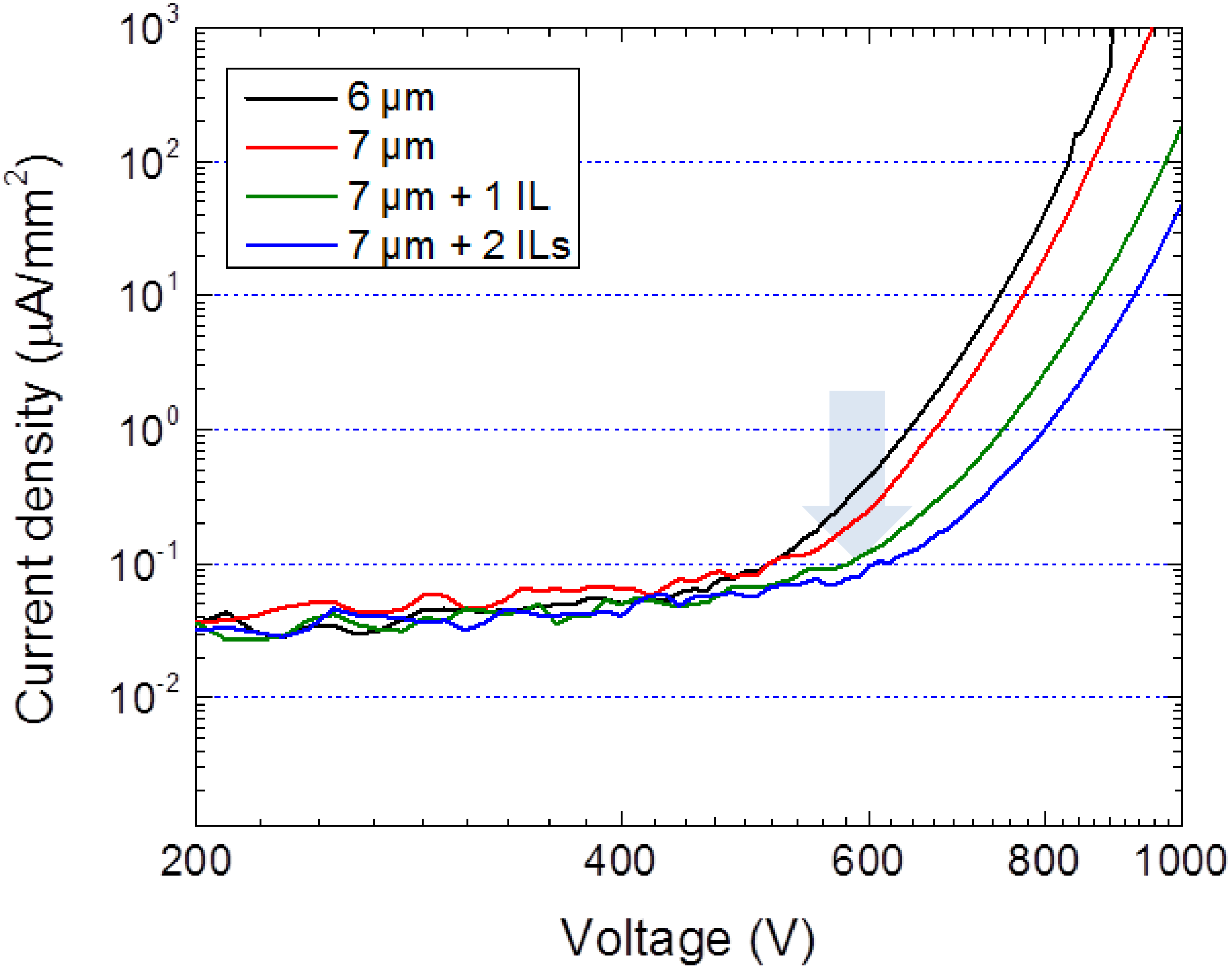
**Interlayer** ▬

**Sample B**
6 µm

**Sample E**
7 µm

**Sample F**
7 µm+1 IL

**Sample G**
7 µm+2 ILs



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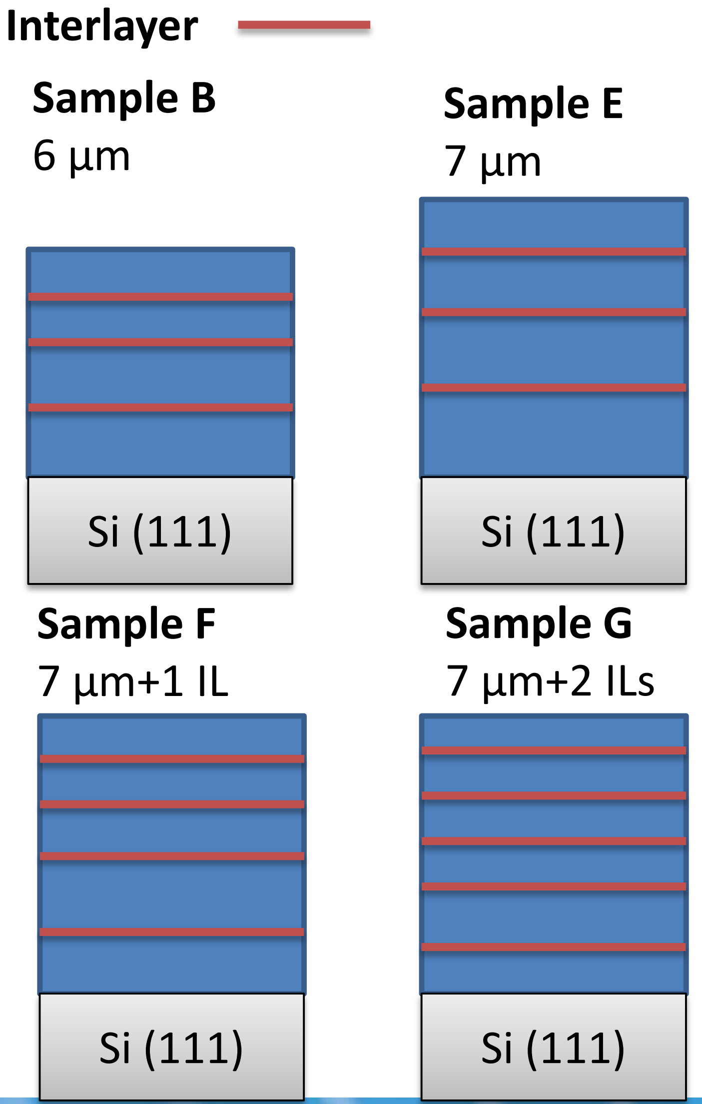
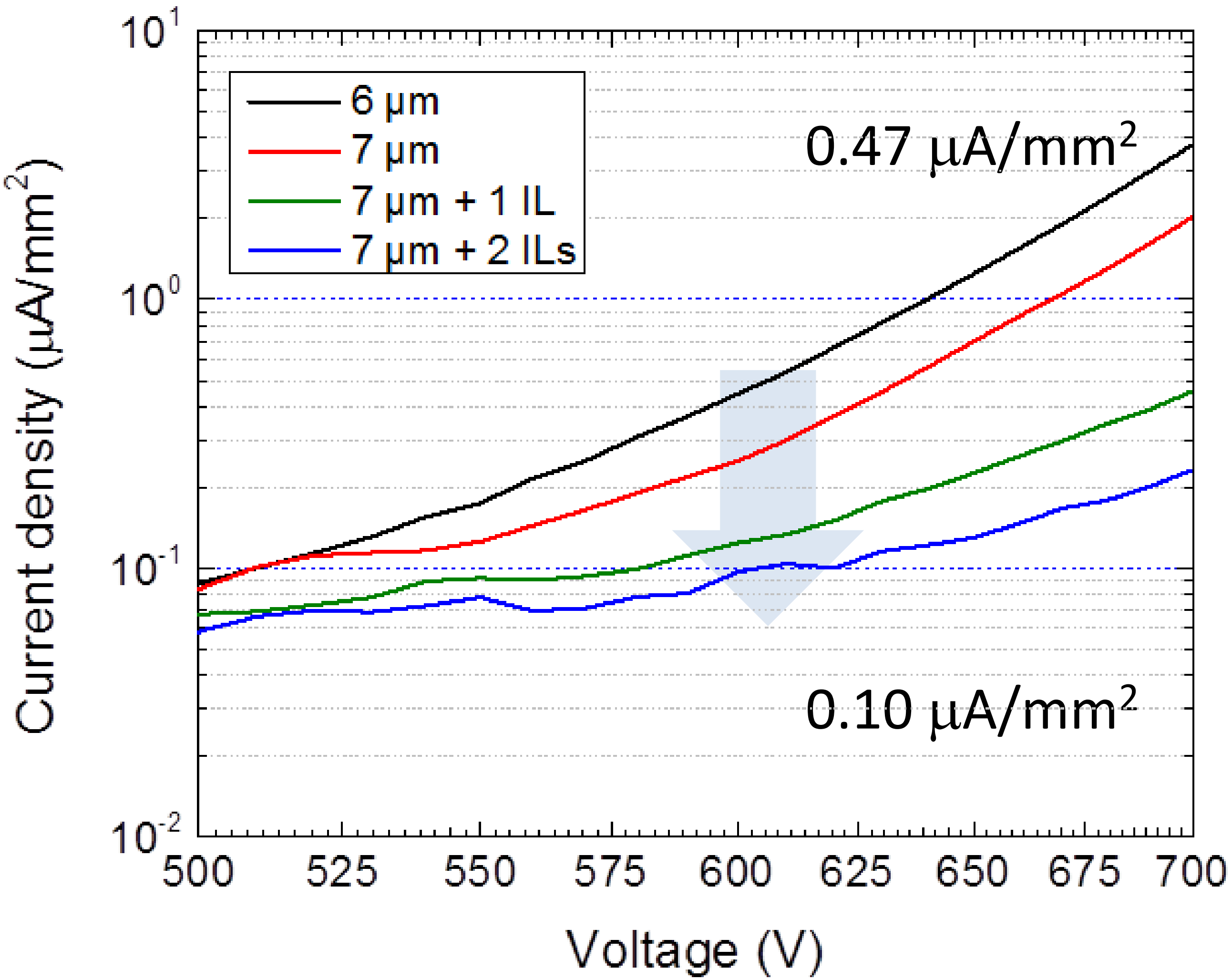
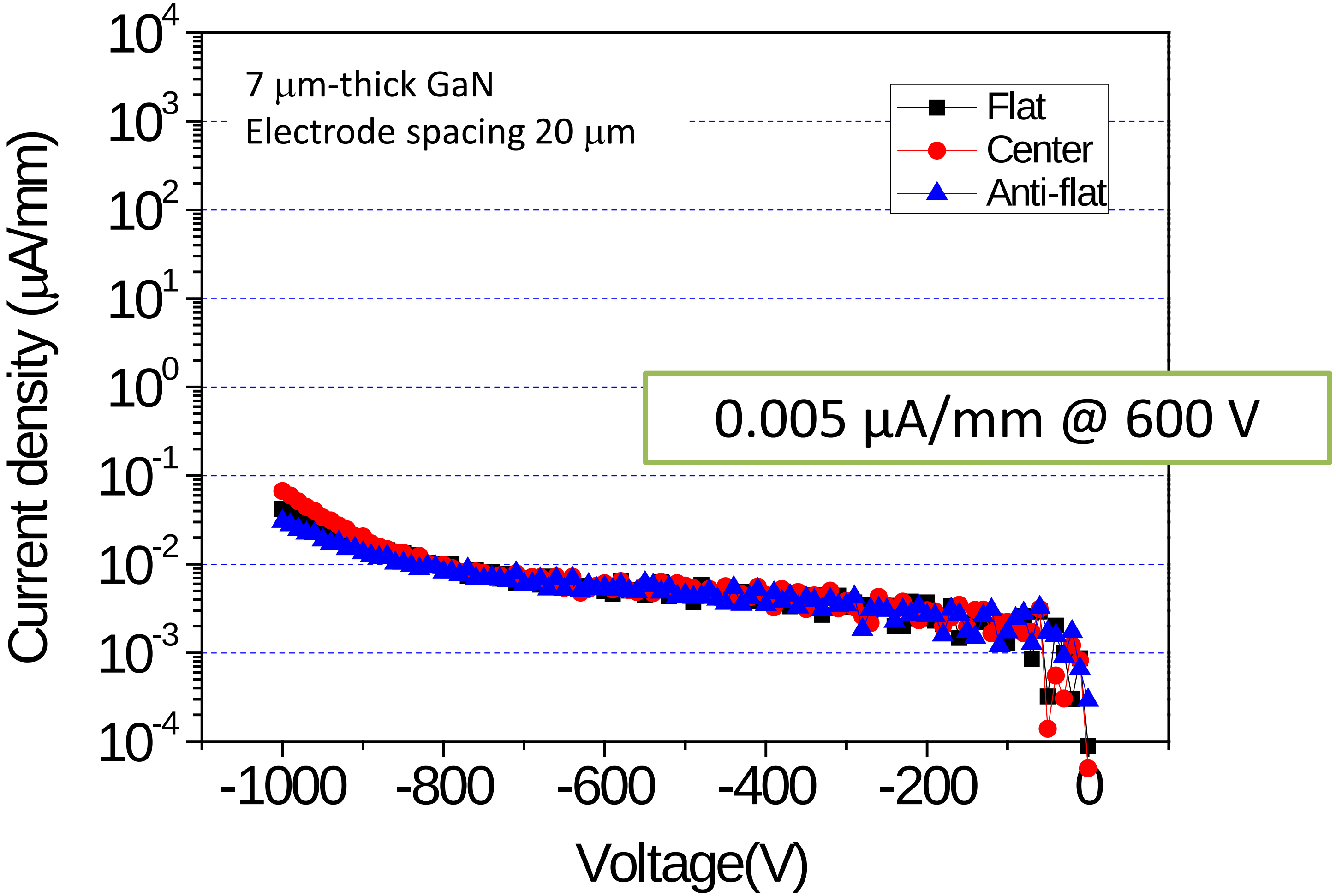




# High crystal quality and low vertical leakage also improve lateral leakage to 0.005 µA/mm @ 600 V

I-V curves of lateral grounded $V_{BR}$ measurement



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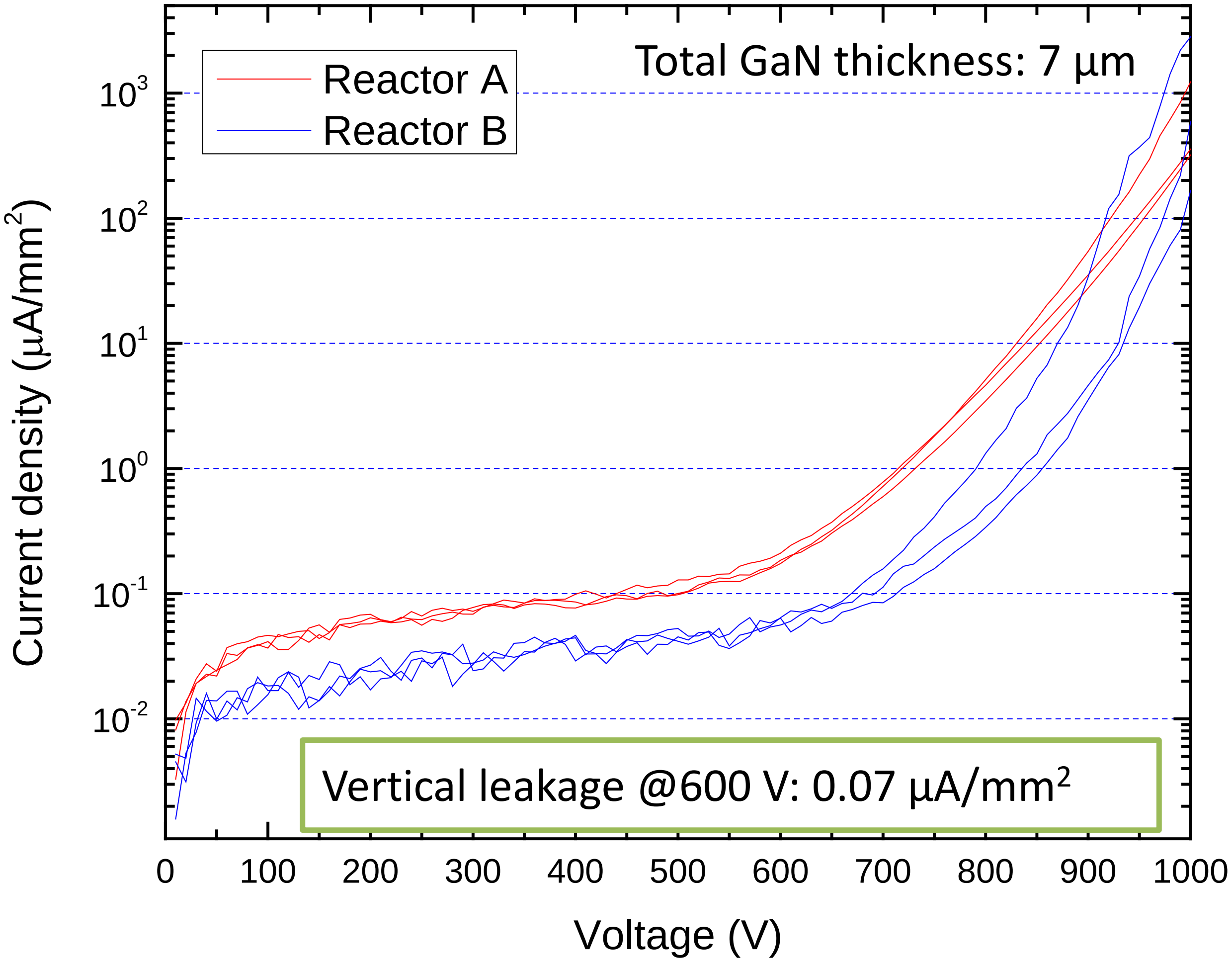
| ~~*“You need carbon doping”*~~ | No – you can have very high isolation based on high-crystal quality and thick GaN. |
| ~~*“Interlayers are bad for leakage”*~~ | The opposite is true: Intelligently designed interlayers suppress the carrier multiplication process in the structure |
| ~~*„The choice of the right reactor is decisive”*~~ | Good hardware matters, however, the same structure with similar material and electrical properties can be grown on different reactors |

# ALLOS can grow the same structure on different reactors with similar results

| | **Reactor A** | **Reactor B** |
|---|---|---|
| Average XRD (002) | 316 arcsec | 348 arcsec |
| Average XRD (102) | 413 arcsec | 416 arcsec |
| Thickness uniformity | 1.11% | 1.32% |
| Mobility | 1950 $cm^2/Vs$ | 2000 $cm^2/Vs$ |



Vertical leakage @600 V: 0.07 $\mu A/mm^2$

# Conclusion: Very low leakage current of 0.07 µA/mm² at 600 V was achieved without doping

**You don't need doping to get high isolation**

- Very high-crystal quality GaN (316 and 413 arcsecs for (002) and (102) XRD respectively)
- 7 µm thickness
- No intentional carbon or other doping in GaN

**Intelligently designed interlayers suppress leakage**

- It is important how to design and grow interlayers
- Electrical performance can be optimized by position and amount of interlayers

**The same structure can be grown on different reactors**

- Similar material and electrical properties achieved on different reactors
- Low leakage current results from ALLOS' structure independent of the reactor

**Thank you very much for your attention!**

**I am happy to take any questions now or after the session and please contact me for any enquiries you may have:**

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**… and do not forget to let me know if you want to receive your public copy of the presentation**