2th November 2017
Session P207

Precise strain-control and excellent emission uniformity of 200 mm GaN-on-Si LED epiwafer for micro LED applications

ALLOS Semiconductors GmbH

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Photo by Seth Doyle on Unsplash

No need to take photos – just email me and get a copy of this presentation

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Outline

A. Strain-control related requirements for micro LED epiwafers

B. Strain-management by AlGaN interlayer

C. Demonstrated results on 200 mm GaN-on-Si for micro LED epiwafers

ALLOS is a fabless IP licensing and technology company

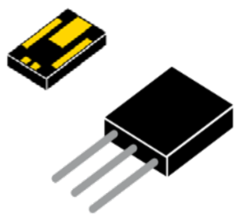
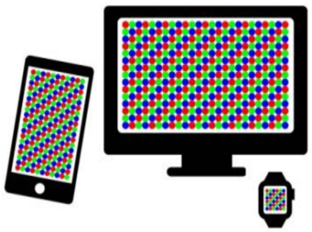
Based on 18 years GaN-on-Si track record at University Magdeburg, AZZURRO and ALLOS

ALLOS enables customers to master GaN-on-Si epiwafer technology

We are continuously improving our technology to stay ahead

Establish 150 and 200 mm GaN-on-Si technology for all applications on customers' reactors

ALLOS' leading GaN-on-Si epiwafer technology is available for all four major market segments

HPE	RF	Micro LED	LED
			
GaN-on-Si enables more efficient high power electronic devices out of silicon lines	GaN-on-Si provides higher performance and lower cost for RF devices	Only GaN-on-Si can deliver the super-uniform, CMOS-compatible large epi-wafers needed for micro LEDs	GaN-on-Si is a niche today but very high cost saving potential remains attractive for the future

Why do people look at micro LED displays?

Display Technology	LCD	OLED	Micro LED
Mechanism	Backlight / LED	Self-emissive	Self-emissive
Contrast Ratio	5,000:1	∞	∞
Lifespan	Medium	Medium	Long
Response Time	ms	μs	ns
Operating Temperature	-40 to 100°C	-30 to 85°C	-100 to 120°C
Power Consumption	High	Medium	Low
View Angle	Low	Medium	High
Pixel per inch	Up to 800 ppi	500 ppi	>2000 ppi
Cost	Low	Medium	High

Source: LEDinside

Why do micro LED displays require a quantum leap in manufacturing?

- A simple 4K UHD display has 3,840 x 2,160 pixels (= 8,294,400)
- Using RGB will require more than 24,800,000 micro LED chips

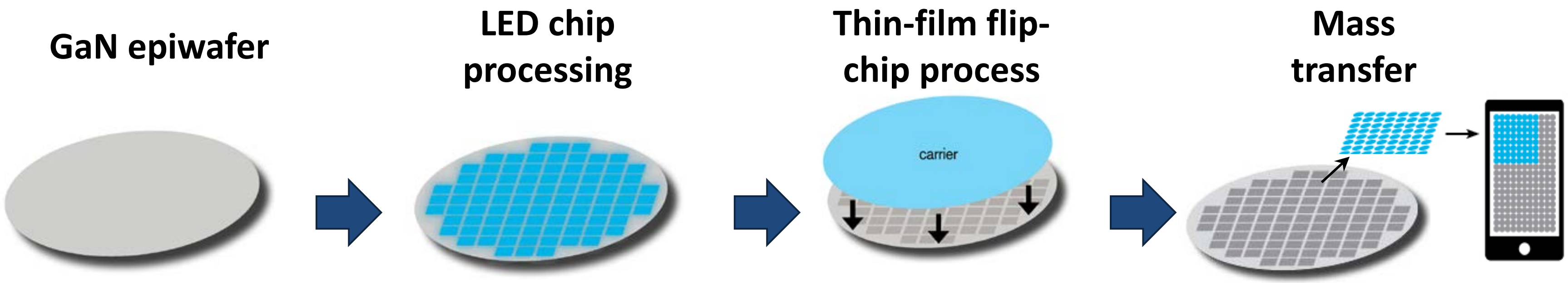
Relevant yield*	… equals amount of chips failing
90.00000 %	2,488,320.00
95.00000 %	1,244,160.00
99.00000 %	248,832.00
99.90000 %	24,883.20
99.99000 %	2,488.32
99.99900 %	248.83
99.99990 %	24.88
99.99999 %	2.49

Even a **Six Sigma = 99.99 % defect-free process will require 2,488 chips to be repaired on a 4K UHD display**

- Today consumers do not accept pixel errors
- Even with *extremely high yield* a repair strategy is unavoidable

* Combined yield of all processes including on-wafer yield, LED chip making yield, transfer yield, etc.

The relevant yield results from all process steps

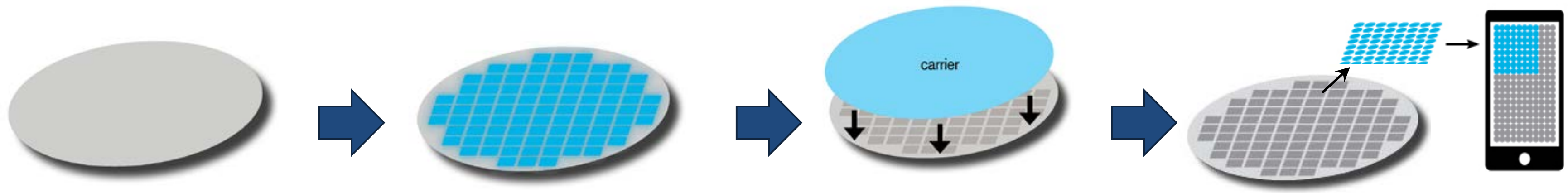


Good area x Good LEDs on wafer x Good LEDs after bonding and substrate removal x Transfer yield

$$= \frac{\text{Good LEDs on display}^{*}}{\text{LEDs transferred to display}}$$

* before repair

Wafer properties determine cost and yield in later manufacturing steps



Large Wafer diameter	Sharp decrease of cost per chip	Sharp decrease of cost per chip	Better wafer area utilization for given stamp size
Flat wafers	Needed to process large wafers	Higher bonding yield	
No cracks, no residual strain	Very low breakage	Higher bonding yield	
High crystal quality	High emission effi-ciency and reliability		
Excellent emission uniformity	On-wafer yield is approaching “1 bin”		Mass transfer of large areas possible with minimal repair need

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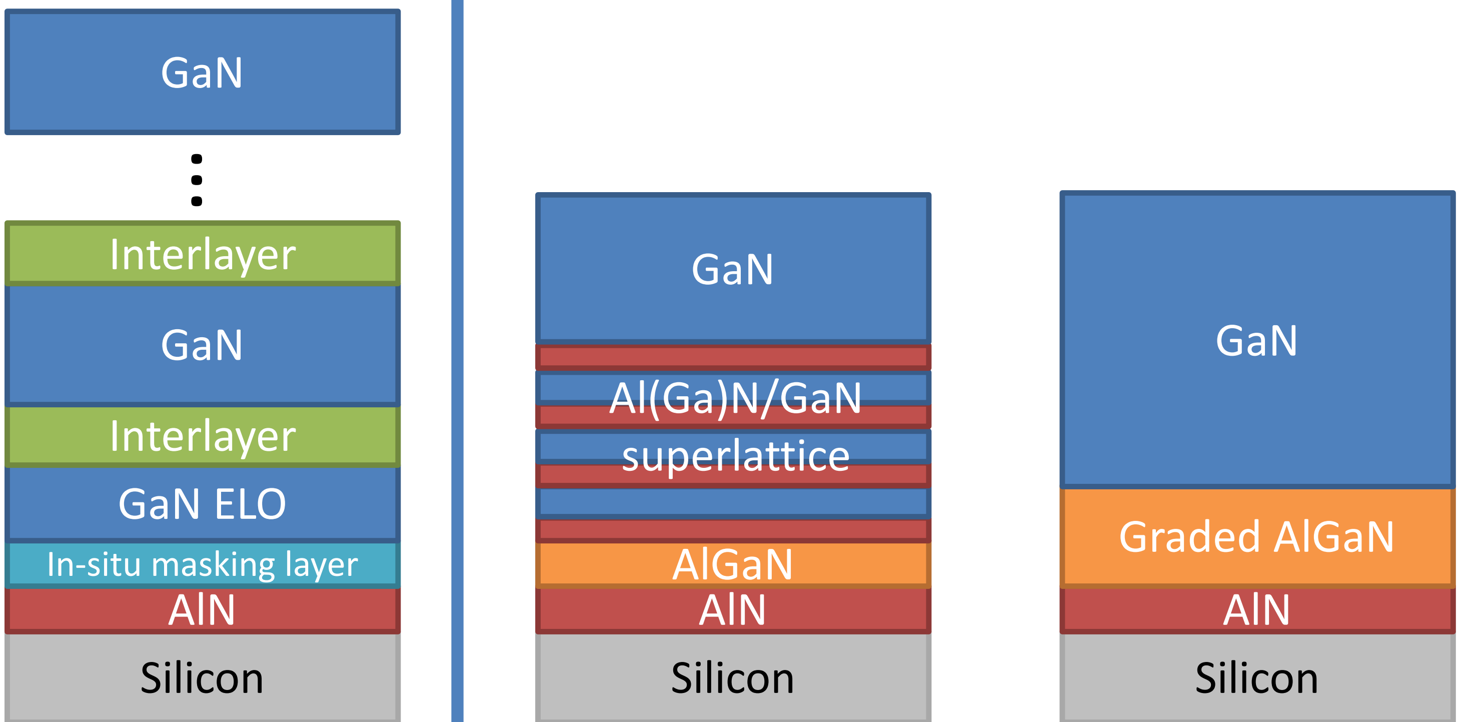
ALLOS' strain-management is based on nucleation layer and interlayers

GaN ELO + interlayers | **Superlattice buffer** | **Graded AlGaN buffer**



University Magdeburg, AZZURRO and ALLOS Semiconductors

Nagoya Institute of Technology

Nitronex

The decisive role of strain-engineering

Control strain through interlayers → Strain-engineering

Strain-engineering →
- Large Wafer diameter
- Flat wafers
- No cracks, no residual strain
- Excellent emission uniformity
- Thick GaN layer → High crystal quality

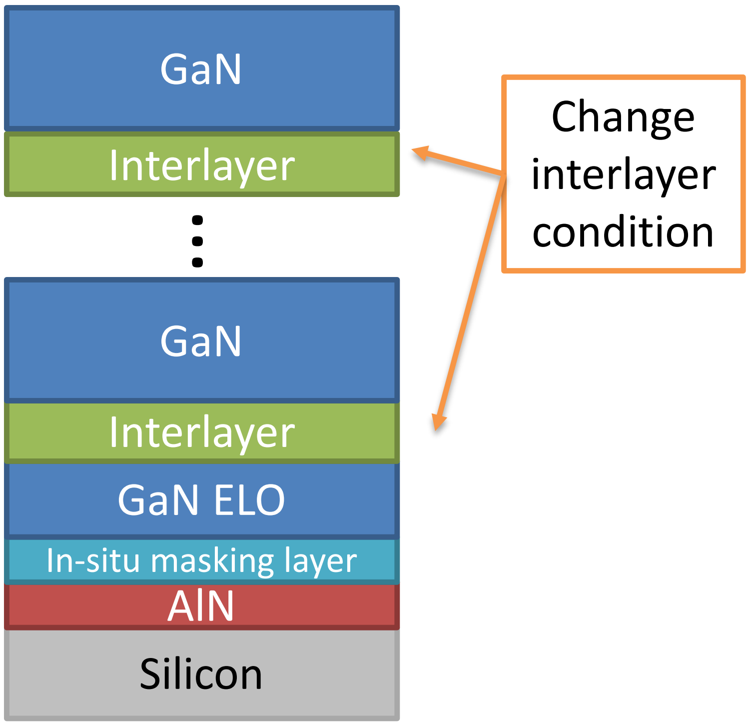
Applied method

This work shows how to control the strain very precisely by IL composition

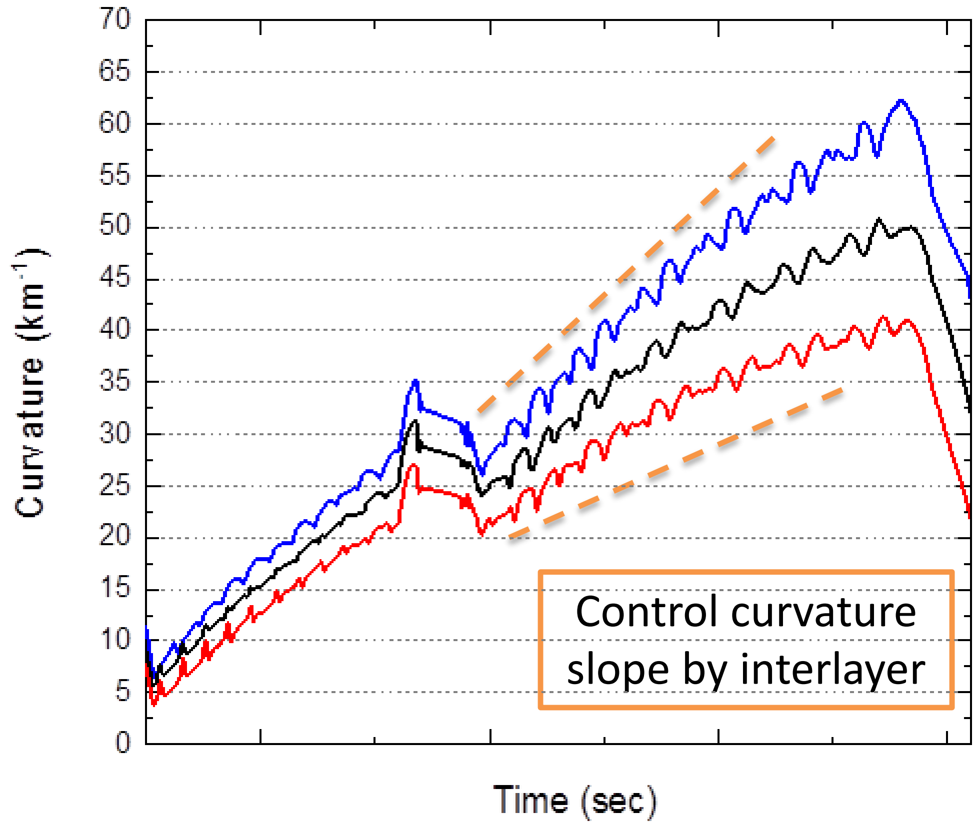
Previously used method

Control strain mainly by IL thickness or IL growth temperature

ALLOS' strain-control technology allows to target different bow levels



Curvature profile during n-GaN growth with different interlayer growth conditions



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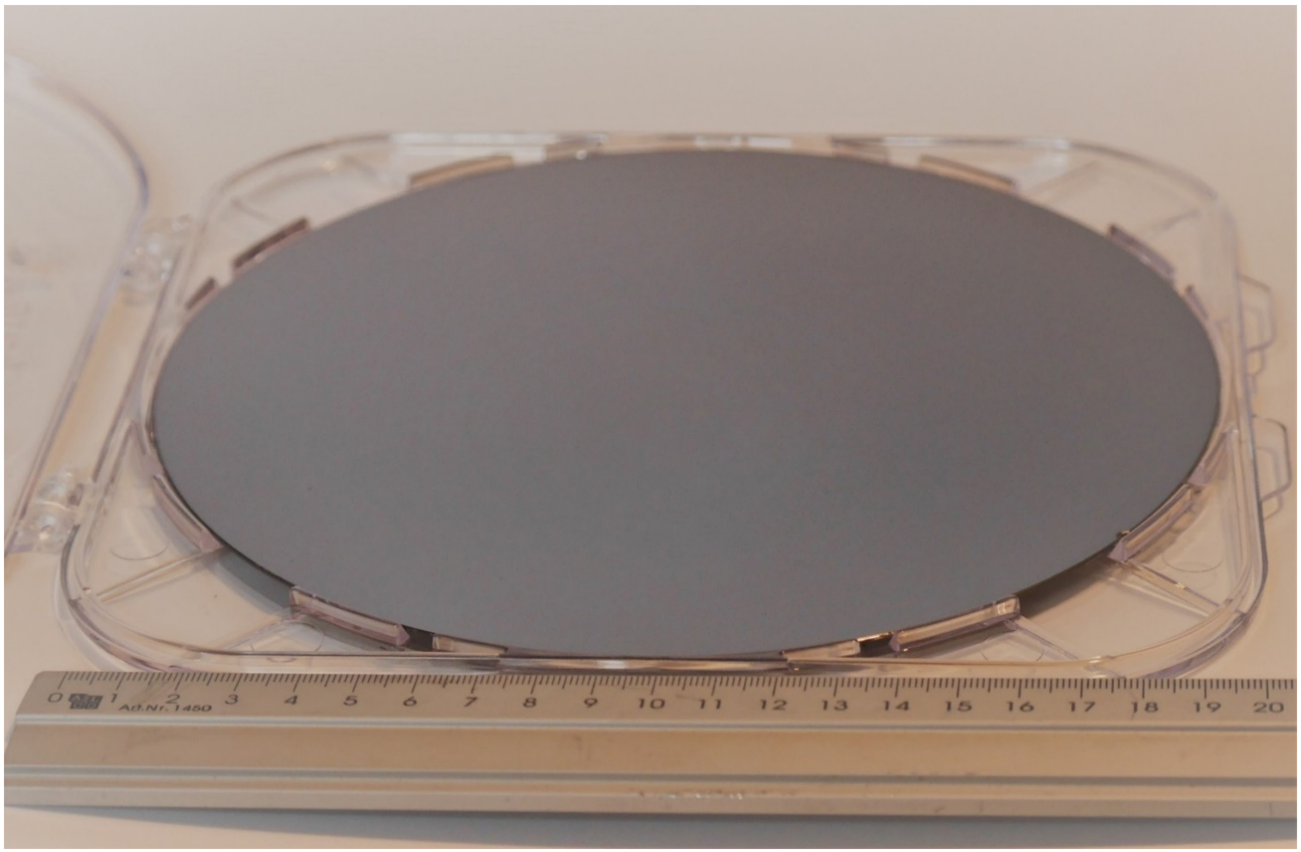
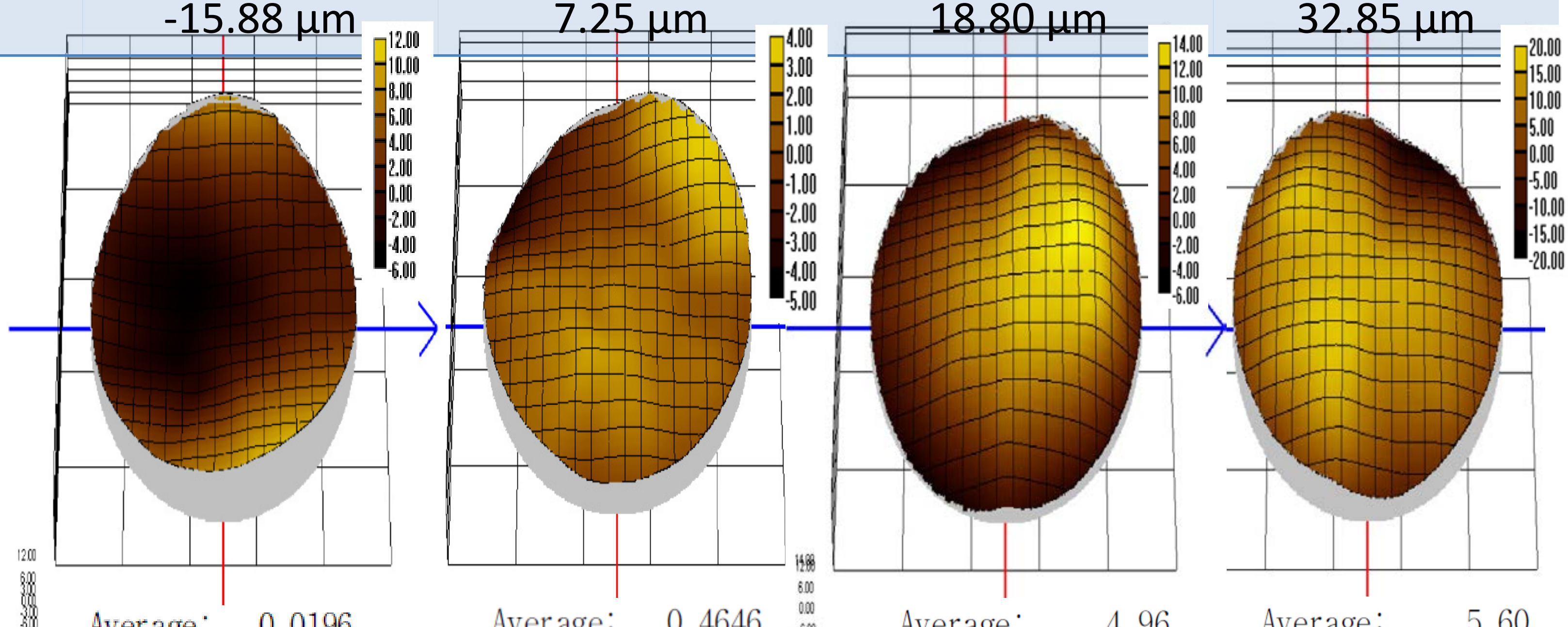
ALLOS' strain-management is successfully applied to 200 mm GaN-on-Si micro LED epiwafer



- Large Wafer diameter ✓
- Flat wafers ✓
- No cracks, no residual strain ✓
- High crystal quality ✓
- Excellent emission uniformity ✓

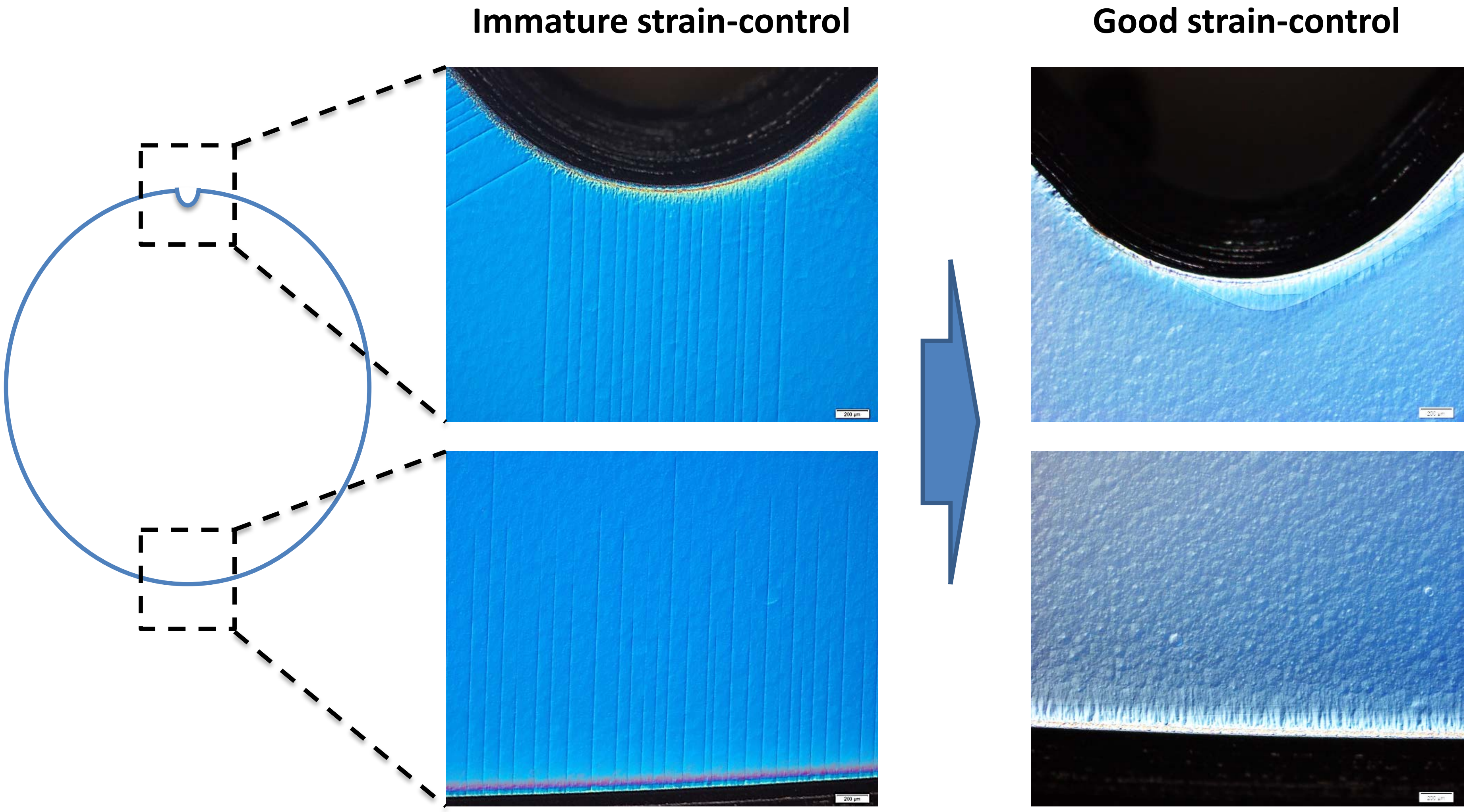
Epiwafer warp (bow) after growth is well-controlled below 30 µm by interlayer growth condition

Max curv. of n-GaN	44.9 km^{-1}	46.3 km^{-1}	48.2 km^{-1}	52.5 km^{-1}
Warp @ RT	-15.88 µm	7.25 µm	18.80 µm	32.85 µm



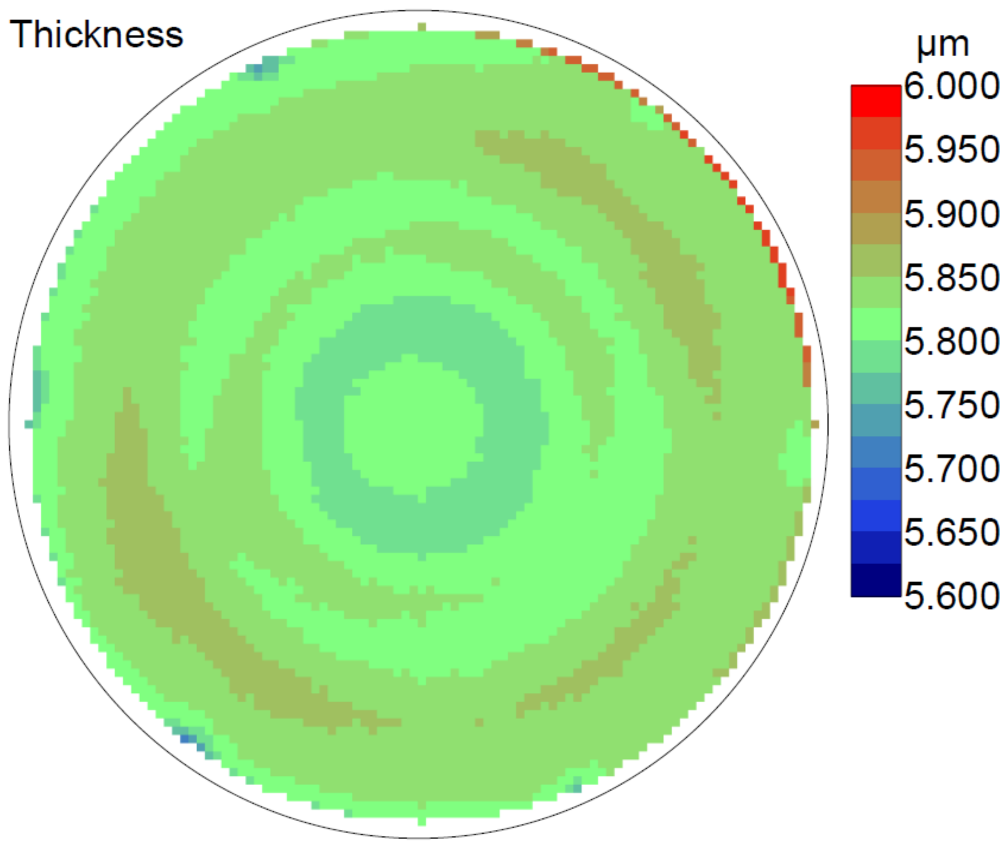
Average:	0.0196	0.4646	4.96	5.60
Minimum:	-5.87	-4.12	-5.17	-17.42
Maximum:	10.01	3.13	13.63	15.43
Std Dev:	3.49	1.28	4.81	6.79

Edge cracks are eliminated even at epiwafer notch with mature strain-engineering



Strain-management allows growth of thick epi layers with excellent uniformity

Thickness mapping of n-GaN buffer of 200 mm LED epiwafer



Statistics

Average	:	5.828 µm
Std dev	:	0.018 µm (0.307 %)
Median	:	5.832 µm

High crystal quality based on thick epi layers and ALLOS' unique buffer growth technology

FWHM of GaN-on-Si LED epiwafer

	Point from center of wafer	FWHM (arcsec)
XRD (002)	0 mm	407
	45 mm	409
	90 mm	388
XRD (102)	0 mm	506
	45 mm	545
	90 mm	494

The current XRD homogeneity level is considered to be sufficient. However, it can be optimized further if needed.

Surface morphology of n-GaN buffer

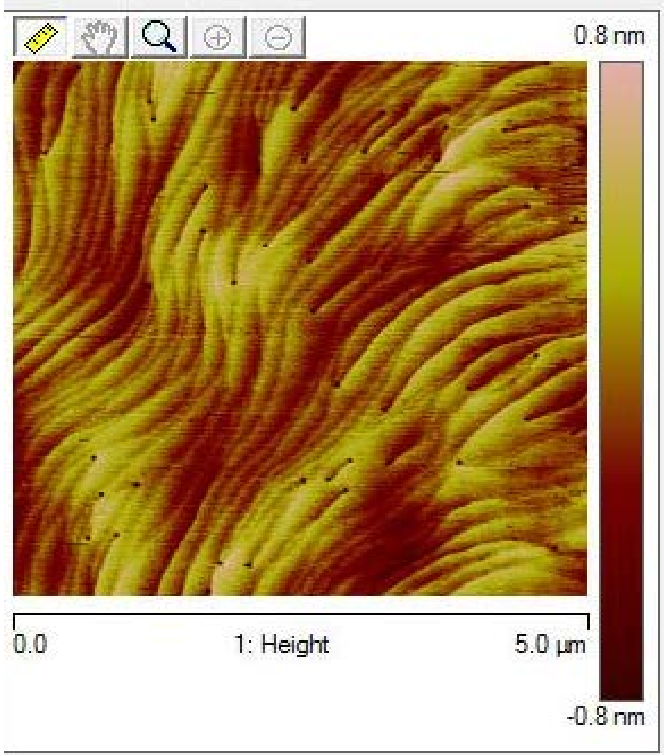
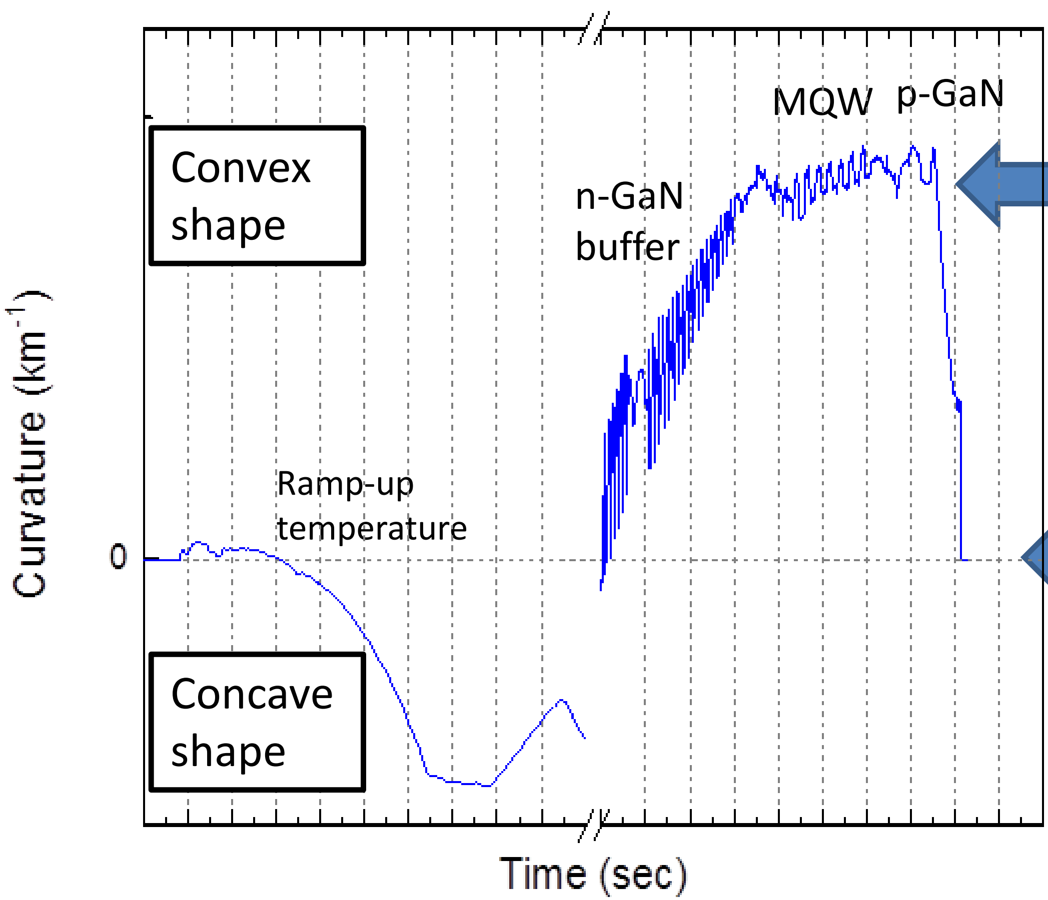


Image Rq	0.216 nm
Image Ra	0.169 nm
Image Rmax	2.99 nm

Strain-engineering can ensure optimal conditions for MQW growth and flat wafer after cooling down

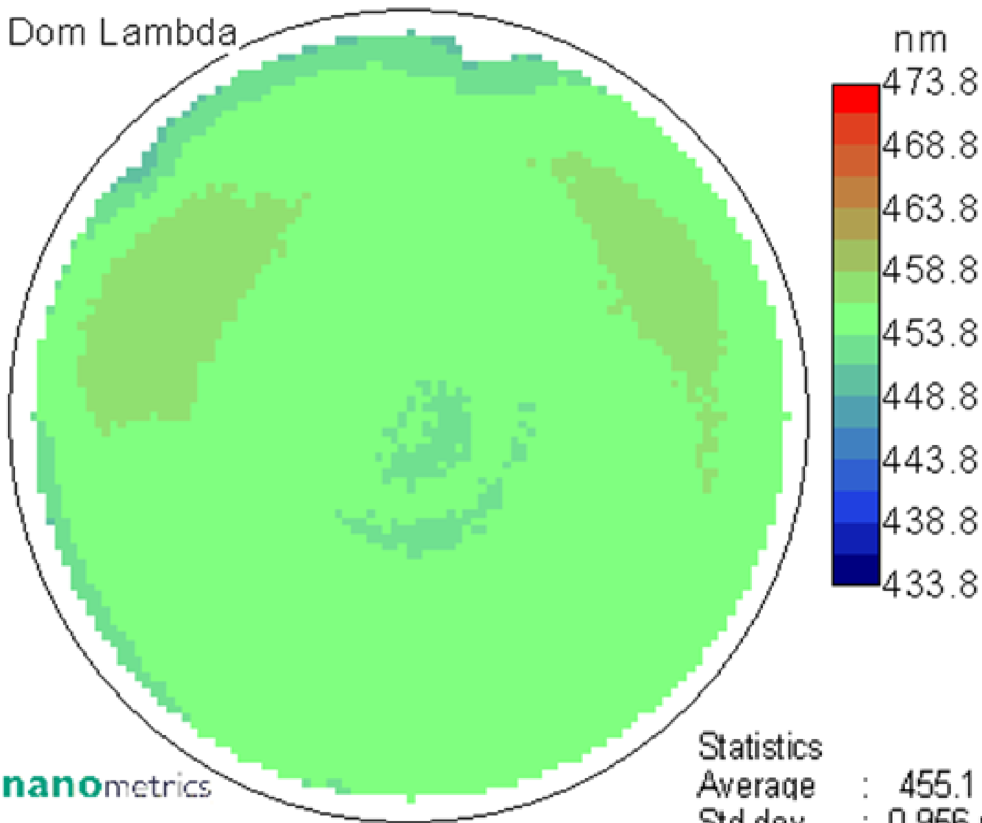
Curvature profile for GaN-on-Si LED growth



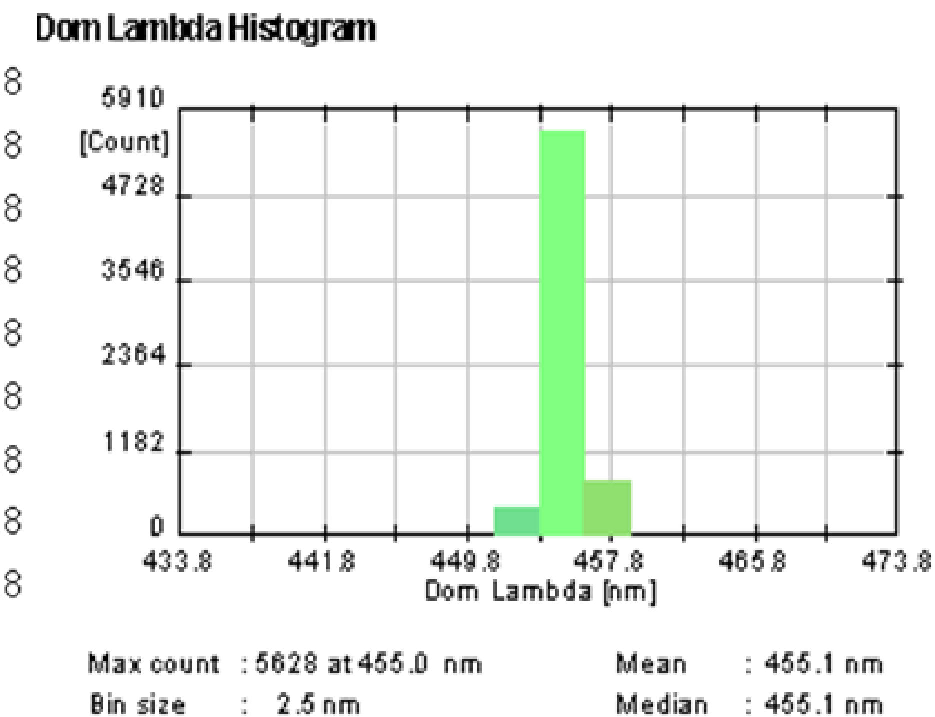
MQW growth with compressive strain

Curvature ~ 0 km^{-1} after cooling down to RT

Excellent emission uniformity < 1 nm is achieved on 200 mm GaN-on-Si micro LED epiwafer



Statistics
Average : 455.1 nm
Std dev : 0.956 nm
(0.210 %)
Median : 455.1 nm
Min : 452.0 nm
Max : 457.6 nm



82.7% in 2.5 nm bin
99.0% in 5.0 nm bin

Conclusion

- Precise strain-control for GaN-on-Si epiwafers is achieved
- This allows to achieve epiwafer values which are crucial for micro LEDs‘ performance, quality and yield:
  - 200 mm diameter GaN-on-Si LED epiwafer
  - Flat wafer
  - Avoid cracks, even at the edge and no residual strain
  - Achieve high crystal quality for 5.8 µm thick epi stack
  - Emission uniformity < 1 nm is achieved
- At the same time the applied strain-engineering does not have any negative side-effect on other epiwafer properties

Thank you very much for your attention!

I am happy to take any questions now or after the session and please contact me for any enquiries you may have or for your copy of the presentation:

BS@allos-semiconductors.com

Don’t miss our joint press release with Veeco Inc. from 01.11.2017 on the same topic.