Precise strain-control and excellent emission uniformity of 200 mm GaN-on-Si LED epiwafer for micro LED applications

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No need to take photos – just email me and get a copy of this presentation

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Outline

A. Strain-control related requirements for micro LED epiwafers

B. Strain-management by AlGaN interlayer

C. Demonstrated results on 200 mm GaN-on-Si for micro LED epiwafers
ALLOS is a fabless IP licensing and technology company.

Based on 18 years GaN-on-Si track record at University Magdeburg, AZZURRO and ALLOS.

ALLOS enables customers to master GaN-on-Si epiwafer technology.

We are continuously improving our technology to stay ahead.

Establish 150 and 200 mm GaN-on-Si technology for all applications on customers’ reactors.
ALLOS’ leading GaN-on-Si epiwafer technology is available for all four major market segments.

- **HPE**: GaN-on-Si enables more efficient high power electronic devices out of silicon lines.
- **RF**: GaN-on-Si provides higher performance and lower cost for RF devices.
- **Micro LED**: Only GaN-on-Si can deliver the super-uniform, CMOS-compatible large epi-wafers needed for micro LEDs.
- **LED**: GaN-on-Si is a niche today but very high cost saving potential remains attractive for the future.
Why do people look at micro LED displays?

<table>
<thead>
<tr>
<th>Display Technology</th>
<th>LCD</th>
<th>OLED</th>
<th>Micro LED</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mechanism</td>
<td>Backlight / LED</td>
<td>Self-emissive</td>
<td>Self-emissive</td>
</tr>
<tr>
<td>Contrast Ratio</td>
<td>5,000:1</td>
<td>∞</td>
<td>∞</td>
</tr>
<tr>
<td>Lifespan</td>
<td>Medium</td>
<td>Medium</td>
<td>Long</td>
</tr>
<tr>
<td>Response Time</td>
<td>ms</td>
<td>µs</td>
<td>ns</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>-40 to 100°C</td>
<td>-30 to 85°C</td>
<td>-100 to 120°C</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>High</td>
<td>Medium</td>
<td>Low</td>
</tr>
<tr>
<td>View Angle</td>
<td>Low</td>
<td>Medium</td>
<td>High</td>
</tr>
<tr>
<td>Pixel per inch</td>
<td>Up to 800 ppi</td>
<td>500 ppi</td>
<td>&gt;2000 ppi</td>
</tr>
<tr>
<td>Cost</td>
<td>Low</td>
<td>Medium</td>
<td>High</td>
</tr>
</tbody>
</table>

Source: LEDinside
Why do micro LED displays require a quantum leap in manufacturing?

- A simple 4K UHD display has 3,840 x 2,160 pixels (= 8,294,400)
- Using RGB will require more than 24,800,000 micro LED chips

<table>
<thead>
<tr>
<th>Relevant yield*</th>
<th>... equals amount of chips failing</th>
</tr>
</thead>
<tbody>
<tr>
<td>90.00000 %</td>
<td>2,488,320.00</td>
</tr>
<tr>
<td>95.00000 %</td>
<td>1,244,160.00</td>
</tr>
<tr>
<td>99.00000 %</td>
<td>248,832.00</td>
</tr>
<tr>
<td>99.90000 %</td>
<td>24,883.20</td>
</tr>
<tr>
<td>99.99000 %</td>
<td>2,488.32</td>
</tr>
<tr>
<td>99.99900 %</td>
<td>248.83</td>
</tr>
<tr>
<td>99.99990 %</td>
<td>24.88</td>
</tr>
<tr>
<td>99.99999 %</td>
<td>2.49</td>
</tr>
</tbody>
</table>

Even a Six Sigma = 99.99 % defect-free process will require 2,488 chips to be repaired on a 4K UHD display.

- Today consumers do not accept pixel errors
- Even with extremely high yield a repair strategy is unavoidable

* Combined yield of all processes including on-wafer yield, LED chip making yield, transfer yield, etc.
The relevant yield results from all process steps

GaN epiwafer → LED chip processing → Thin-film flip-chip process → Mass transfer

Good area × Good LEDs on wafer × Good LEDs after bonding and substrate removal × Transfer yield

= Good LEDs on display*

LEDs transferred to display

* before repair
Wafer properties determine cost and yield in later manufacturing steps

- **GaN epiwafer**
- **LED chip processing**
- **Thin-film flip-chip process**
- **Mass transfer**

<table>
<thead>
<tr>
<th>Benefit</th>
<th>Sharp decrease of cost per chip</th>
<th>Sharp decrease of cost per chip</th>
<th>Better wafer area utilization for given stamp size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Large Wafer diameter</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Flat wafers</td>
<td>Needed to process large wafers</td>
<td>Higher bonding yield</td>
<td></td>
</tr>
<tr>
<td>No cracks, no residual strain</td>
<td>Very low breakage</td>
<td>Higher bonding yield</td>
<td></td>
</tr>
<tr>
<td>High crystal quality</td>
<td>High emission efficiency and reliability</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Excellent emission uniformity</td>
<td>On-wafer yield is approaching “1 bin”</td>
<td></td>
<td>Mass transfer of large areas possible with minimal repair need</td>
</tr>
</tbody>
</table>
Outline

A. Strain-control related requirements for micro LED epiwafers

B. Strain-management by AlGaN interlayer

C. Demonstrated results on 200 mm GaN-on-Si for micro LED epiwafers
ALLOS’ strain-management is based on nucleation layer and interlayers

GaN ELO + interlayers

Superlattice buffer

Graded AlGaN buffer

University Magdeburg, AZZURRO and Nagoya Institute of Technology

Nagoya Institute of Technology

Nitronex
The decisive role of strain-engineering

Applied method
This work shows how to control the strain very precisely by IL composition

Previously used method
Control strain mainly by IL thickness or IL growth temperature
ALLOS’ strain-control technology allows to target different bow levels

Curvature profile during n-GaN growth with different interlayer growth conditions

- Change interlayer condition
- Control curvature slope by interlayer
Outline

A. Strain-control related requirements for micro LED epiwafers

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C. Demonstrated results on 200 mm GaN-on-Si for micro LED epiwafers
ALLOS’ strain-management is successfully applied to 200 mm GaN-on-Si micro LED epiwafer

- Large Wafer diameter
- Flat wafers
- No cracks, no residual strain
- High crystal quality
- Excellent emission uniformity
Epiwafer warp (bow) after growth is well-controlled below 30 µm by interlayer growth condition

<table>
<thead>
<tr>
<th>Max curvature of n-GaN</th>
<th>44.9 km(^{-1})</th>
<th>46.3 km(^{-1})</th>
<th>48.2 km(^{-1})</th>
<th>52.5 km(^{-1})</th>
</tr>
</thead>
<tbody>
<tr>
<td>Warp @ RT</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-15.88 µm</td>
<td>0.0196</td>
<td>-5.87</td>
<td>10.01</td>
<td>3.49</td>
</tr>
<tr>
<td>7.25 µm</td>
<td>0.4646</td>
<td>-4.12</td>
<td>3.13</td>
<td>1.28</td>
</tr>
<tr>
<td>18.80 µm</td>
<td>4.96</td>
<td>-5.17</td>
<td>13.63</td>
<td>4.81</td>
</tr>
<tr>
<td>32.85 µm</td>
<td>5.60</td>
<td>-17.42</td>
<td>15.43</td>
<td>6.79</td>
</tr>
</tbody>
</table>
Edge cracks are eliminated even at epiwafer notch with mature strain-engineering

Immature strain-control

Good strain-control
Strain-management allows growth of thick epi layers with excellent uniformity

Thickness mapping of n-GaN buffer of 200 mm LED epiwafer

Statistics
- Average: 5.828 μm
- Std dev: 0.018 μm (0.307 %)
- Median: 5.832 μm
High crystal quality based on thick epi layers and ALLOS’ unique buffer growth technology

### FWHM of GaN-on-Si LED epiwafer

<table>
<thead>
<tr>
<th>XRD (002) Point from center of wafer</th>
<th>FWHM (arcsec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 mm</td>
<td>407</td>
</tr>
<tr>
<td>45 mm</td>
<td>409</td>
</tr>
<tr>
<td>90 mm</td>
<td>388</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>XRD (102) 0 mm</th>
<th>506</th>
</tr>
</thead>
<tbody>
<tr>
<td>45 mm</td>
<td>545</td>
</tr>
<tr>
<td>90 mm</td>
<td>494</td>
</tr>
</tbody>
</table>

The current XRD homogeneity level is considered to be sufficient. However, it can be optimized further if needed.

### Surface morphology of n-GaN buffer

![Surface morphology image](image-url)
Strain-engineering can ensure optimal conditions for MQW growth and flat wafer after cooling down.

Curvature profile for GaN-on-Si LED growth

Convex shape

Ramp-up temperature

n-GaN buffer

MQW p-GaN

Curvature ~ 0 km\(^{-1}\) after cooling down to RT

Concave shape

MQW growth with compressive strain
Excellent emission uniformity < 1 nm is achieved on 200 mm GaN-on-Si micro LED epiwafer

82.7% in 2.5 nm bin
99.0% in 5.0 nm bin
Conclusion

- Precise strain-control for GaN-on-Si epiwafers is achieved
- This allows to achieve epiwafer values which are crucial for micro LEDs’ performance, quality and yield:
  - 200 mm diameter GaN-on-Si LED epiwafer
  - Flat wafer
  - Avoid cracks, even at the edge and no residual strain
  - Achieve high crystal quality for 5.8 µm thick epi stack
  - Emission uniformity < 1 nm is achieved
- At the same time the applied strain-engineering does not have any negative side-effect on other epiwafer properties
Thank you very much for your attention!

I am happy to take any questions now or after the session and please contact me for any enquiries you may have or for your copy of the presentation:

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Don’t miss our joint press release with Veeco Inc. from 01.11.2017 on the same topic.