ALLOS Semiconductors

State of ALLOS' product for 1200 V high power electronics applications

February 2018

Executive summary

- For each target applications ALLOS has specific epi-structures which we call (epiwafer) ‘products’ and in the high power electronics (HPE) market we have two products:

  1) The established 600 V product with low vertical and lateral leakage currents (carbon-doping free)

  2) A 1200 V product which is under development

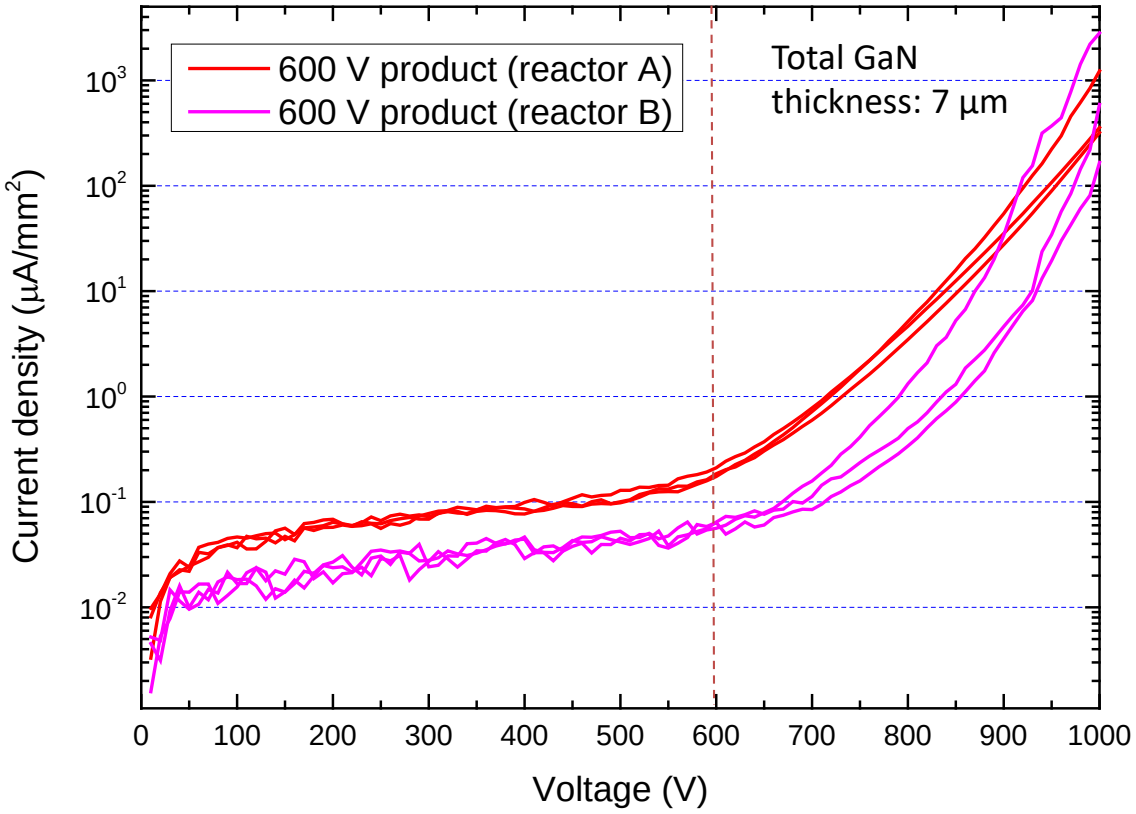
- Purpose of this presentation is to show the state of ALLOS’ product for 1200 V applications and to explain the next development steps
- IEMN recently showed more than 1400 V lateral (grounded) and vertical physical breakdown
- Ongoing 1200 V program combines existing and tested novel technical elements to make the 1200 V product available for interested device makers

ALLOS' technology is available on any MOCVD reactor

Epi structure	600 V product* (reactor A)	600 V product (reactor B)
Average XRD (002)	316 arcsec	348 arcsec
Average XRD (102)	413 arcsec	416 arcsec
Thickness uniformity	1.11 %	1.32 %
Mobility	1950 cm^2/Vs	2000 cm^2/Vs

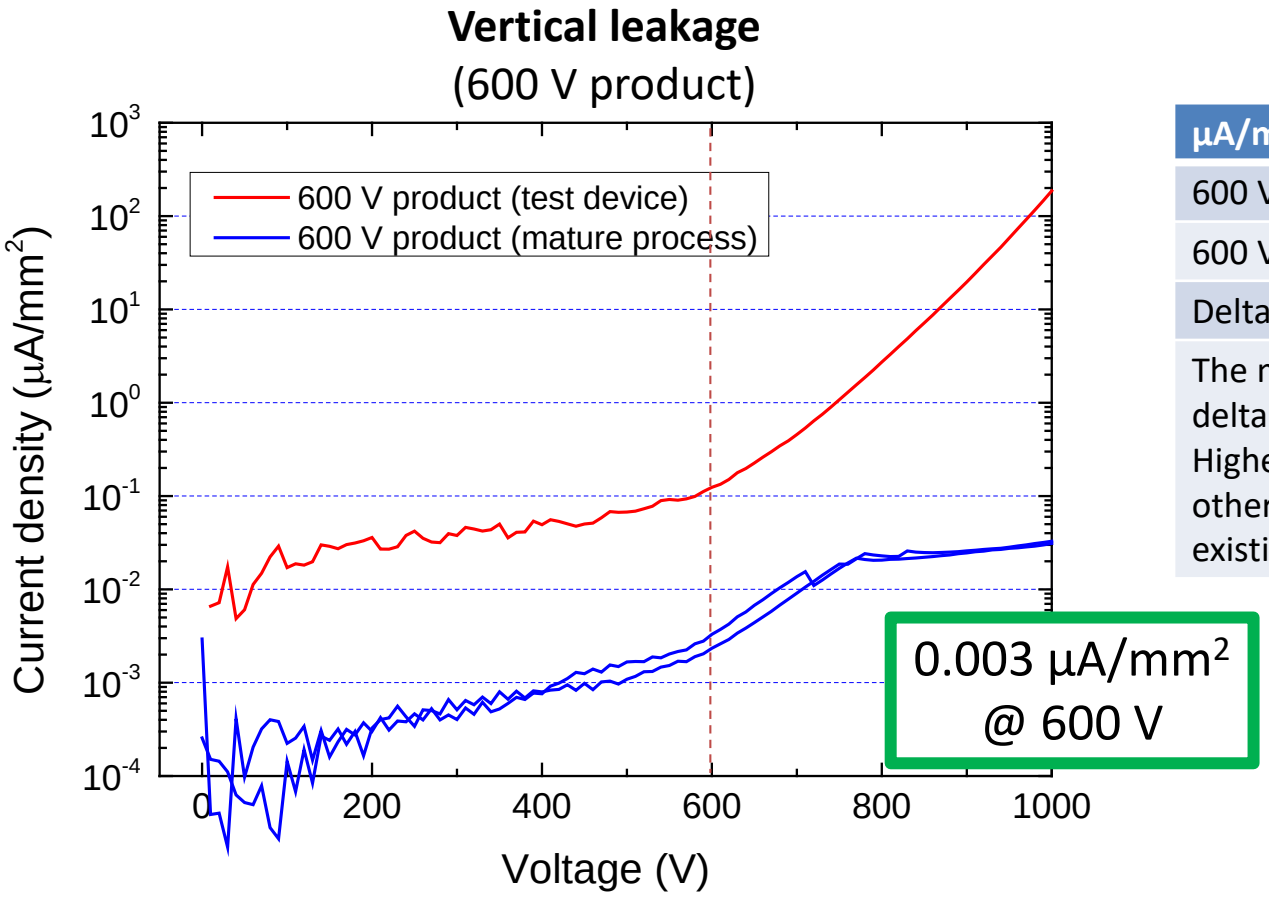
* As a 'reference' line ALLOS' 600 V product grown on reactor A is shown in red color on all the following slides which are showing only ALLOS' results

Vertical leakage
(600 V product)



This page shows project results where the same epi structure (600 V product) was grown on two of the major reactor types from different hardware makers. Objective of the project was to compare the relative performance of the two reactors and to determine the production strategy of the customer. The resulting epiwafers were processed using the same device design on the same process line. Please note that the device processing of the customer used here applied a simplified device design to allow fast feedback on the epi development. Consequently, the leakage is much higher than the performance on mature devices (for that see next slide). All data shown by courtesy of the customer.

Mature device process shows the full performance of ALLOS' 600 V product with very low vertical leakage



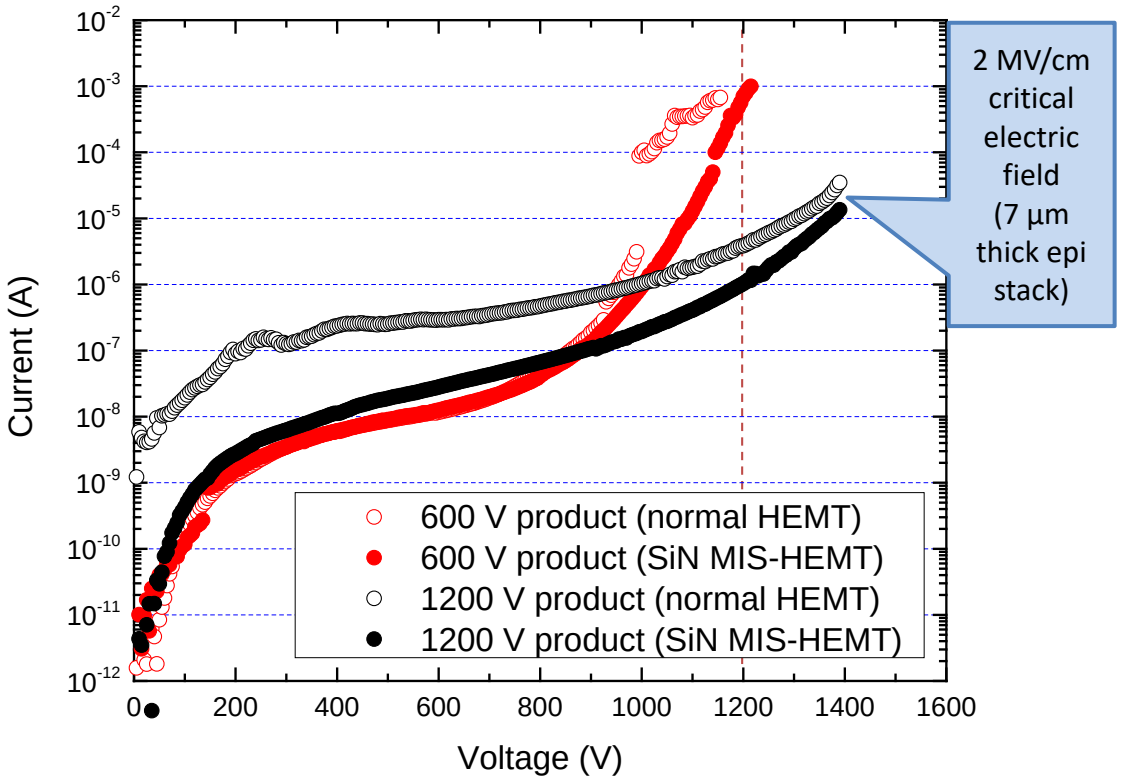
µA/mm²	@ 600 V	@ 1000 V
600 V product (test device)	0.12	190
600 V product (mature process)	0.003	0.033
Delta	- 96 %	> - 99 %

The mature device process offers possible explanations for delta:
Higher quality sidewalls (e. g. implantation vs. MESA) and other processing related influences on isolation (e. g. existing passivation during contact annealing).

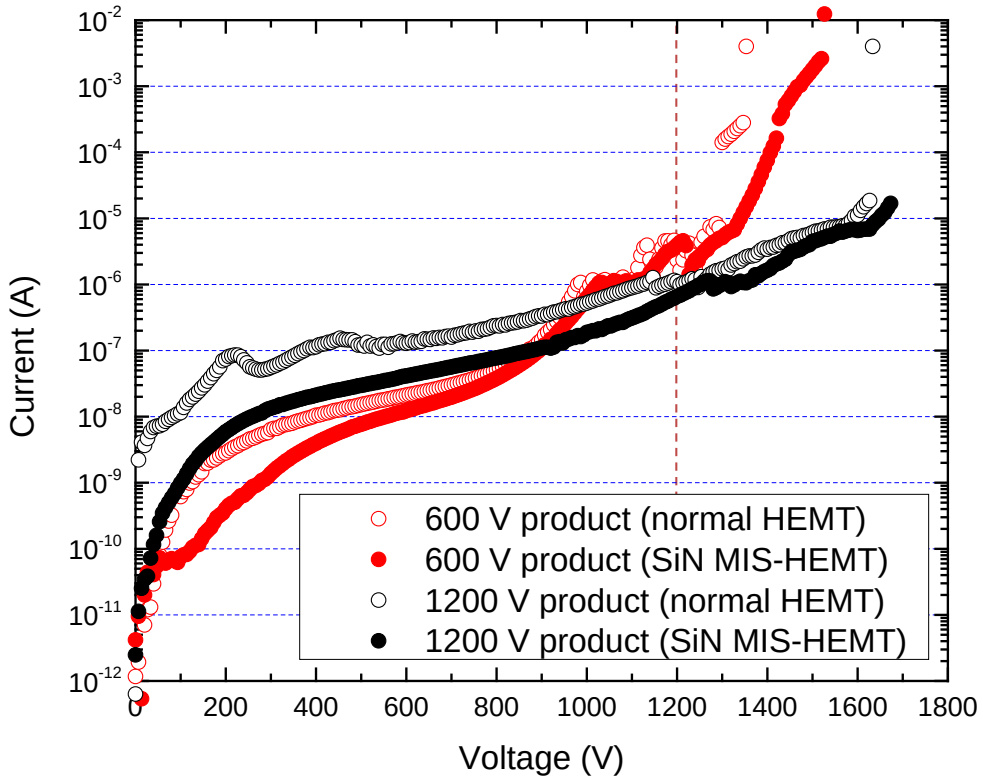
This page shows results from sister-epiwafers (same recipe for 600 V product from reactor A on previous page) with different devices processes. The red 'reference' line shows results from one customer using a simplified structure which allows very fast feedback on epi development (see previous page). The blue line shows results from another customer using a mature device design and process. All data shown by courtesy of the respective customer.

IEMN showed more than 1400 V lateral and vertical physical breakdown on ALLOS' carbon-doping free GaN-on-Si

Vertical breakdown
(600 V and 1200 V products)



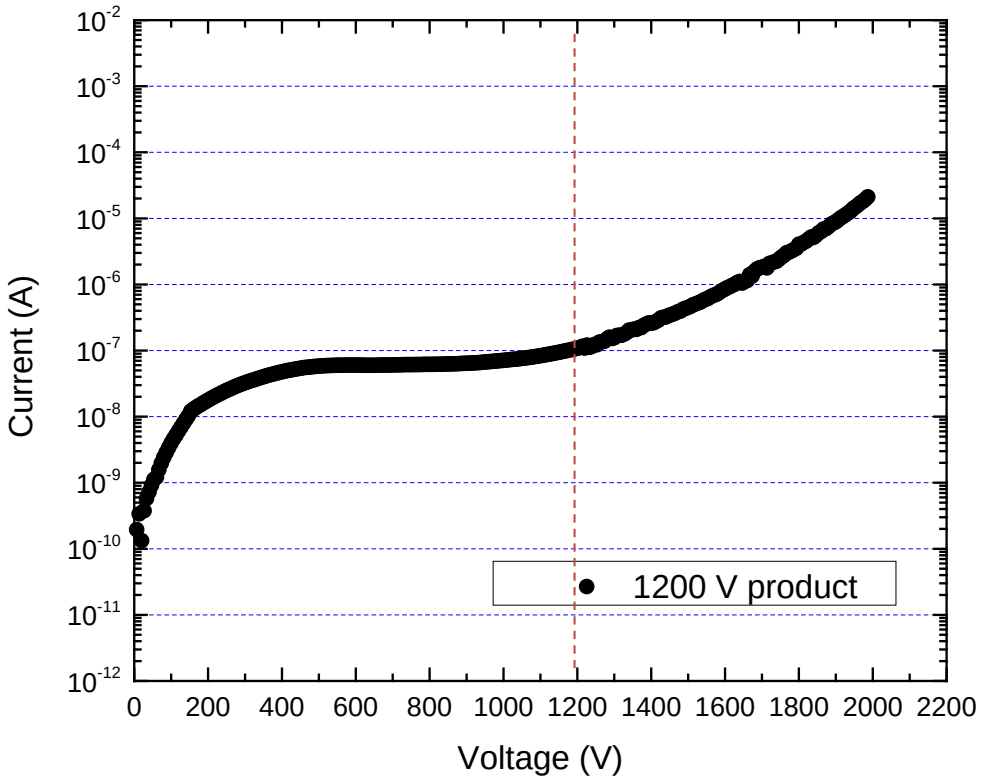
Lateral grounded breakdown
(600 V and 1200 V products)



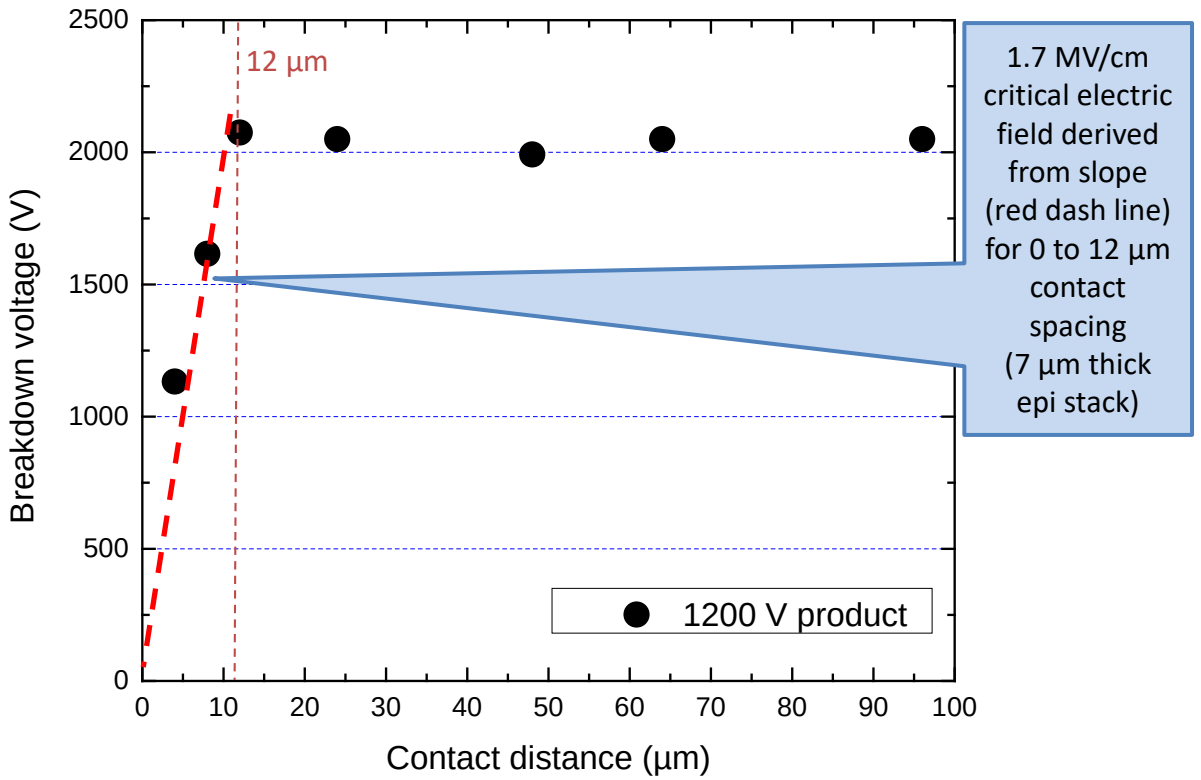
Red 'reference' lines show device data using the same standard epiwafer structure of ALLOS' 600 V product as shown on the previous slides, while the black lines are of the modified structure which is currently under development for 1200 V devices (1200 V product). IEMN has applied two different device making processes (solid and doted lines) and used specialized high voltage measurement equipment. Data by courtesy of Dr. Farid Medjdoub and team at IEMN.

Lateral floating measurement showed 2000 V breakdown and saturation for electrode spacing above 12 µm

Lateral floating breakdown
(1200 V product)



Lateral floating breakdown as a function of electrode spacing (1200 V product)

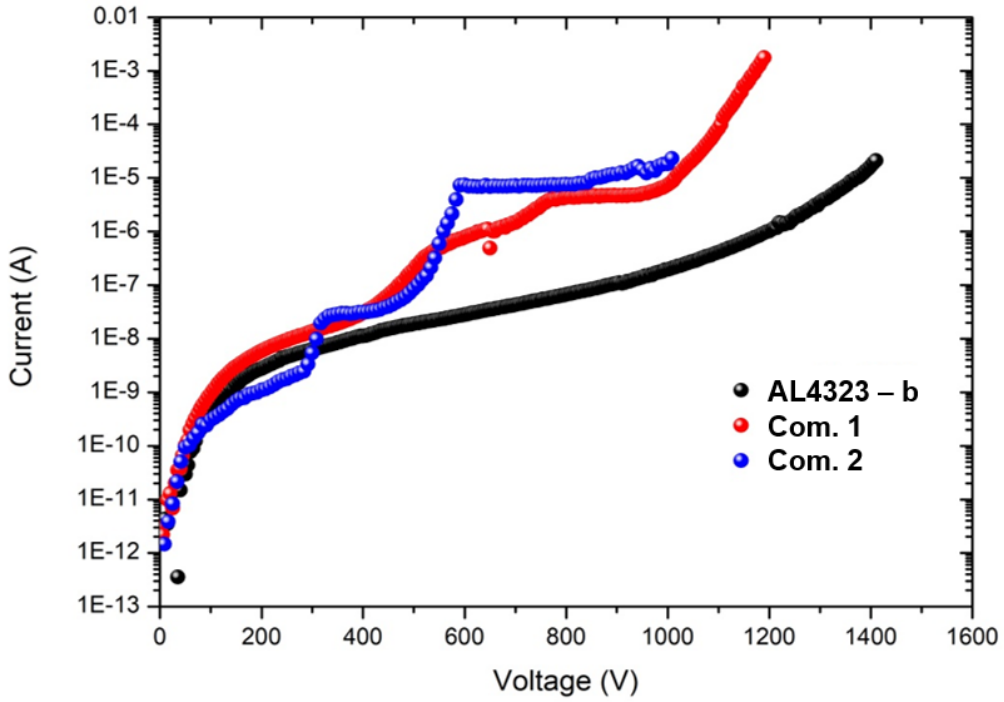


1.7 MV/cm critical electric field derived from slope (red dash line) for 0 to 12 µm contact spacing (7 µm thick epi stack)

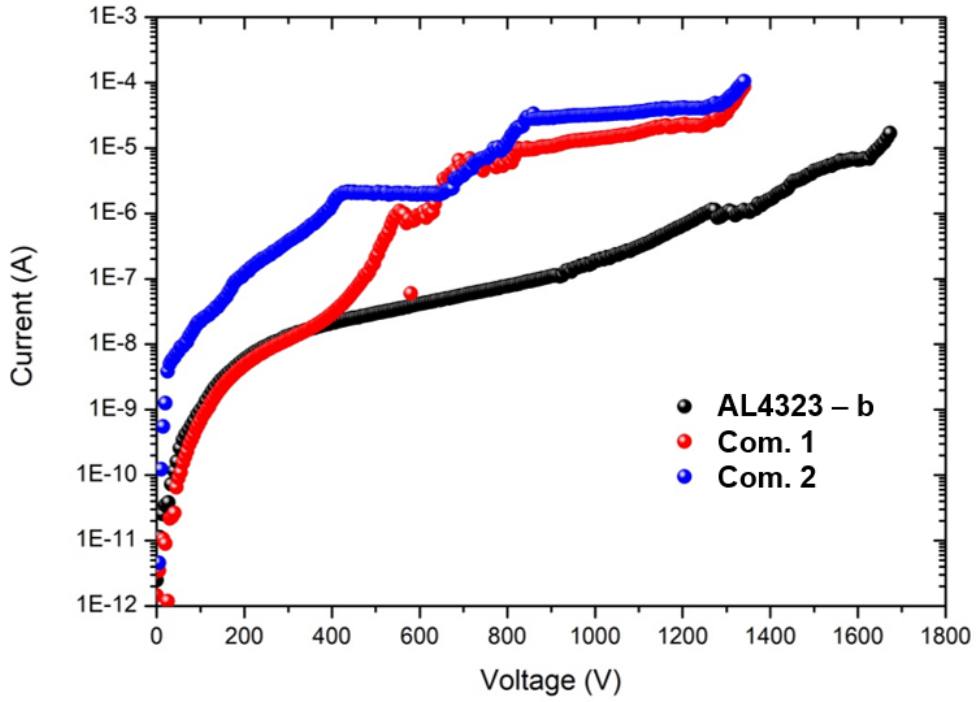
Black lines/points show device data using the same epiwafer of ALLOS' 1200 V product as shown on the previous slide. Data by courtesy of Dr. Farid Medjdoub and team at IEMN.

IEMN showed much better breakdown and leakage characteristics for ALLOS compared with two other major players

Vertical breakdown
(ALLOS' 1200 V product)



Lateral grounded breakdown
(ALLOS' 1200 V product)



Black line is ALLOS' structure modified for 1200 V devices (see previous pages). Red and blue lines are epiwafers from two other leading power semiconductor players. All wafers have been characterized using the same device design, processing and measurement set-up by IEMN. IEMN commented "Significant difference (2 decades lower leakage) in breakdown characteristics compared to other commercial sources". Graphs by courtesy of Dr. Farid Medjdoub and team at IEMN.

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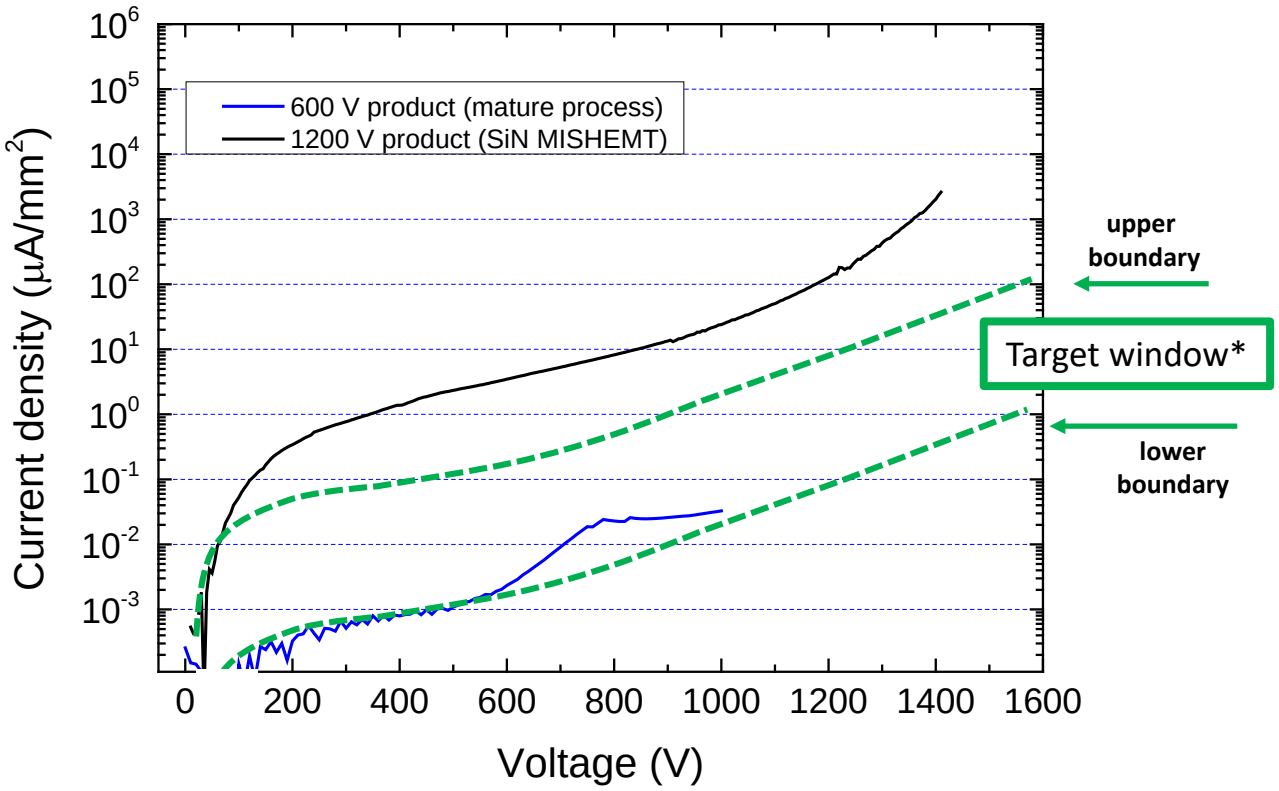
Ongoing 1200 V program combines existing and tested novel technical elements to make the 1200 V product available

Objectives of 1200 V development program:

1. Reduce the leakage further over the entire voltage range
2. Increase the physical breakdown voltage further to improve safety margin
   - Today's performance: > 1400 V
   - Target: stable performance >> 1400 V
3. Maintain the other excellent epiwafer characteristics (see next page)

State of technology and development target (illustration)**



* Expected target window for 1200 V product (upper and lower boundary) depending on device design, device process and measurement setup.
** The 1200 V product results (like black line shown on slide 5) are from device processing with simplified device design to allow fast feedback and from measurement equipment for higher voltages with limitation in lower current resolution. The blue line shows the performance of ALLOS' epiwafer with a mature device design and processing (same results as on slide 4).

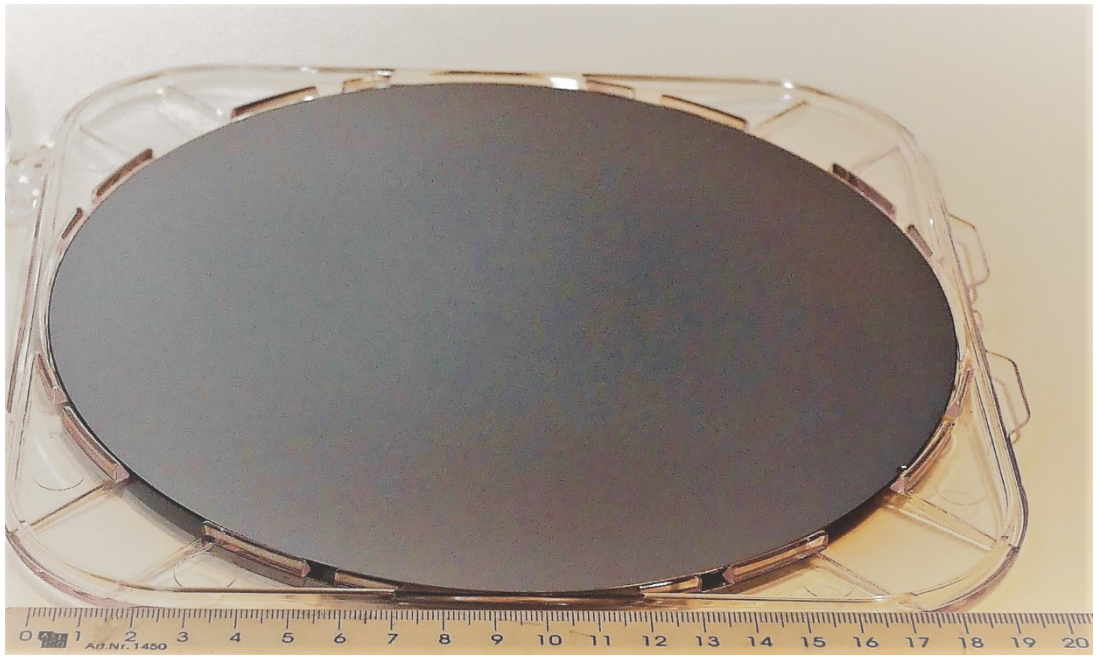
ALLOS' product for 1200 V application meets the same high quality standards like any other epiwafer from ALLOS

Standard epiwafer quality characteristics include:

- Superior crystal quality and very low TDD (2E8/cm^2)
- No cracks, no pits, no meltback
- Available with thicknesses of 625 µm (at 150 mm) and 725 µm (at 200 mm)
- Low and controlled wafer bow < 30 µm
- Excellent thickness uniformity (0.3 % std. dev.) and composition uniformities
- Very good device performance uniformity
- Mobility of 2000 cm^2/Vs and R_{sheet} of 340 Ω/sq.

Like other ALLOS technologies it is available on any MOCVD reactor

Typical 200 mm HPE epiwafer with ALLOS' technology



ALLOS has an ongoing program to achieve the 1200 V objectives by combining existing and tested technical elements

Measures to achieve objectives for 1200 V devices (summary from project plan):

1. Increase thickness
   - Today's thickness is 7 µm; ALLOS strain-engineering allows to increase thickness without creating cracks or increasing bow values
2. Further improve crystal quality
3. Apply different layer designs
   - Based on comprehensive existing research of ALLOS
4. Introduce carbon doping
   - All results shown in this presentation are achieved without using carbon doping
   - For 1200 V operations ALLOS considers to apply a specific novel carbon doping technique to minimize negative side-effects of carbon on crystal quality and dynamic behavior
5. Use advantages from new reactor designs

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Thank you for your attention and your feedback!

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