ALLOS Semiconductors

How can GaN-on-Si compete with SiC in the market for 1200 Volt devices?

Burkhard Slischka

10th April 2018, Brussels

CSindustry awards WINNER

CS INTERNATIONAL CONFERENCE

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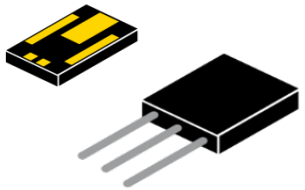
The team of ALLOS Semiconductors

ALLOS' business is to develop and license GaN-on-Si epiwafer technology for three fast-growing markets

High power electronics (HPE)

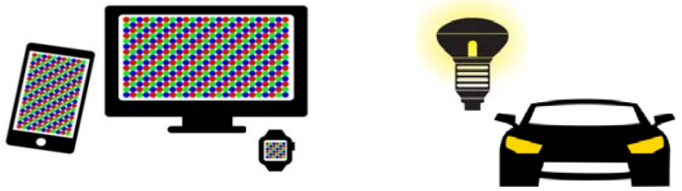


GaN-on-Si enables more energy-efficient, less complex and smaller high power electronic (HPE) devices from existing silicon lines

Radio frequency (RF)

GaN-on-Si provides higher performance, smaller, more energy efficient and lower cost RF devices, for 5G base-stations, smart-phones, CATV, IoT and other RF applications

Micro LED / LED



Only GaN-on-Si allows super-uniform, large diameter, CMOS-compatible "1-bin" epiwafers needed for large-scale micro LED display production

ALLOS* is a leader in GaN-on-Si with a 15 years track-record

end of 90s — GaN-on-Si was pioneered at three places around the world: Nagoya Institute, Nitronex and University of Magdeburg

2003 — AZZURRO founded in Magdeburg and becomes the first epiwafer vendor world-wide

2005 — Products for HPE, RF and LED introduced

2005 — First to show a 150 mm epiwafer

2009 — OSRAM gets license for LED production

2011 — First to offer a commercial 200 mm epiwafer

2011 — AZZURRO closes down

2011 — ALLOS is founded and buys IP and technology for new business model

2013 — Total investment exceeds EUR 40 m

2014 — EPISTAR licenses ALLOS' technology

2015 — Shows leading leakage values and carbon-doping free GaN-on-Si

2016/2017 — VEECO works with ALLOS to show < 1 nm uniformity on 200 mm

2018 — First to show > 1400 V breakdown

* ALLOS and predecessor-company AZZURRO

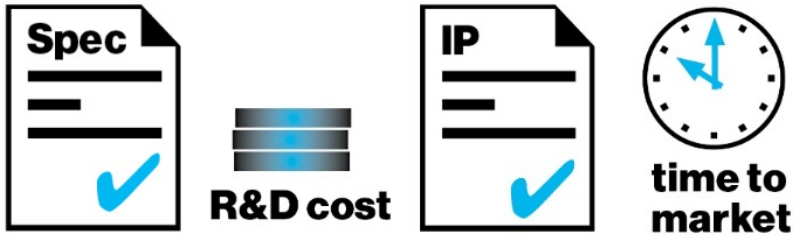
ALLOS' value preposition is to license and transfer turn-key GaN-on-Si epiwafer technology and IP

3 years

Develop GaN-on-Si epitaxy technology by yourself

12 weeks

Work with ALLOS



A. Why is GaN-on-Si limited to 600 V today?

B. What can be achieved with ALLOS' technology?

C. Vision: How to attack SiC with 1200 Volt GaN-on-Si devices?

Overall material properties of GaN are superior to SiC and therefore in theory GaN-on-Si should be better in both performance and cost

Material properties

Parameter	Si	GaAs	4H-SiC	GaN
Bandgap energy (eV)	1.12	1.43	3.26	**3.39**
E_c (critical electric field MV/cm)	0.3	0.4	2.5	**3.3**
Electron mobility (cm^2/Vs)	1400	8500	~1020 (1)	**~2000** (2)
Thermal conductivity (W/cmK)	1.5	0.5	**4.9**	2.0
Baliga's FOM = $e\mu E_c^3$	1	16	340	**653**

(1) Mobility depends on SiC orientation
(2) For lateral devices in 2DEG

Theoretically possible device performance

GaN > SiC > Si

Device cost

GaN-on-Si < SiC < GaN-on-GaN

Today's insufficient levels of isolation limit GaN-on-Si to applications of 600 V and below

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In practice because of a high defect levels E_c values better than 0.3 MV/cm are difficult to achieve without additional doping

Therefore, usually carbon-doping is used for power semiconductor GaN-on-Si to increase the isolation. But this has side-effects

Growing thicker is not an option as typically 4 to 5 µm GaN is the limit

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ALLOS is focusing on thick, un-doped, high-quality GaN

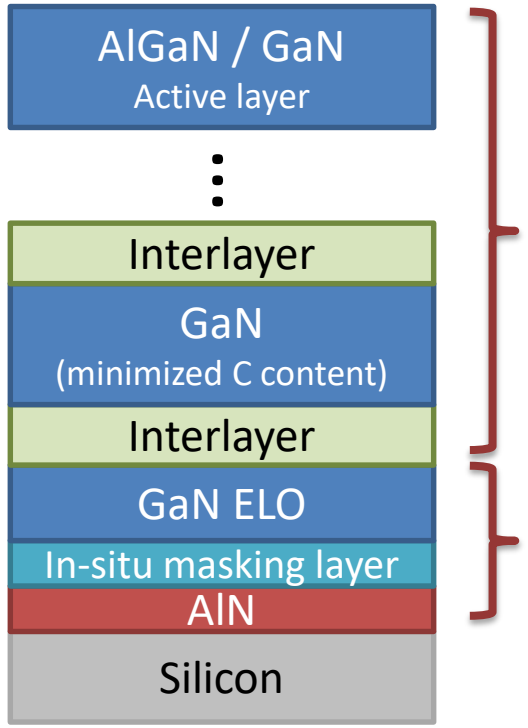
Grow thick

Grow thick (e.g. 7 µm), strain-free and crack-free GaN layers

High quality

Highest crystal quality, undoped GaN [1]

Typical HPE GaN-on-Si structure of ALLOS



Unique IP

Quality improvement

Strain management

Thick GaN layers with several strain-management interlayers [2]

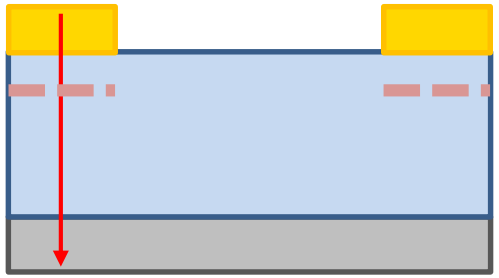
Quality improvement

Epitaxial lateral overgrowth on ALLOS' proprietary in-situ masking layer

[1] For more about ALLOS' results with minimized carbon content see A. Nishikawa, ICNS 2017

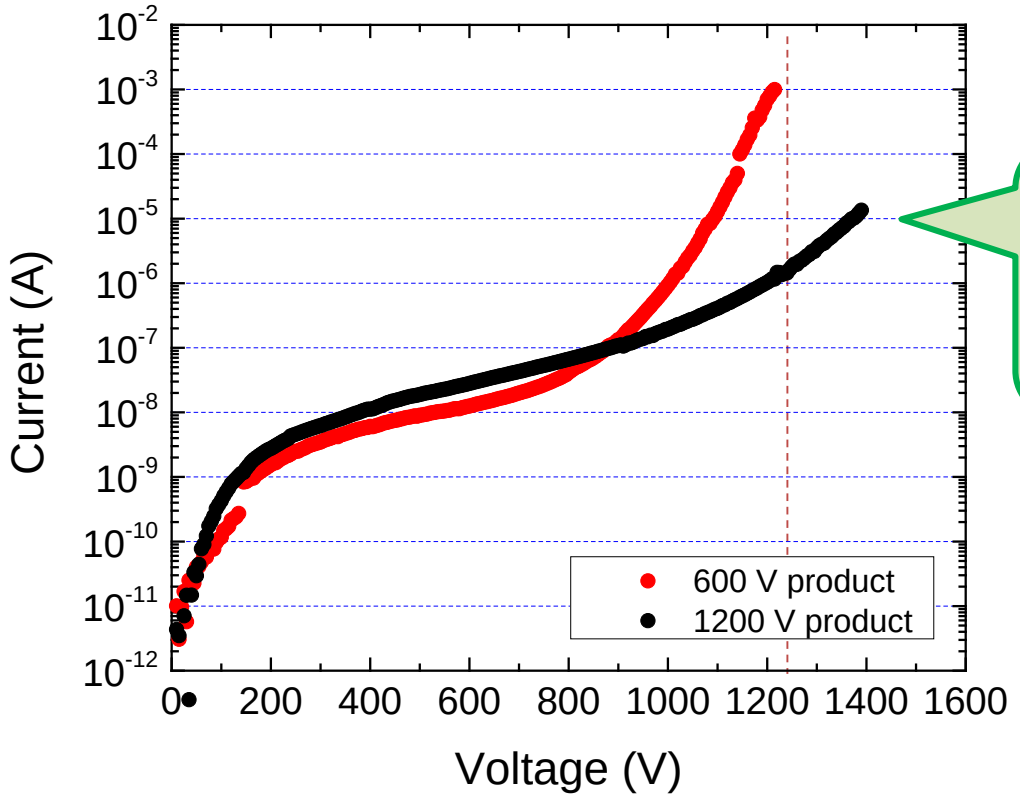
[2] For more about ALLOS' strain engineering see B. Slischka, SSL China 2017

This thick, high quality and optimized GaN stack results in an E_c of 2 MV/cm and a vertical Vbr of over 1400 V for 7 µm thick GaN



2DEG channel disabled

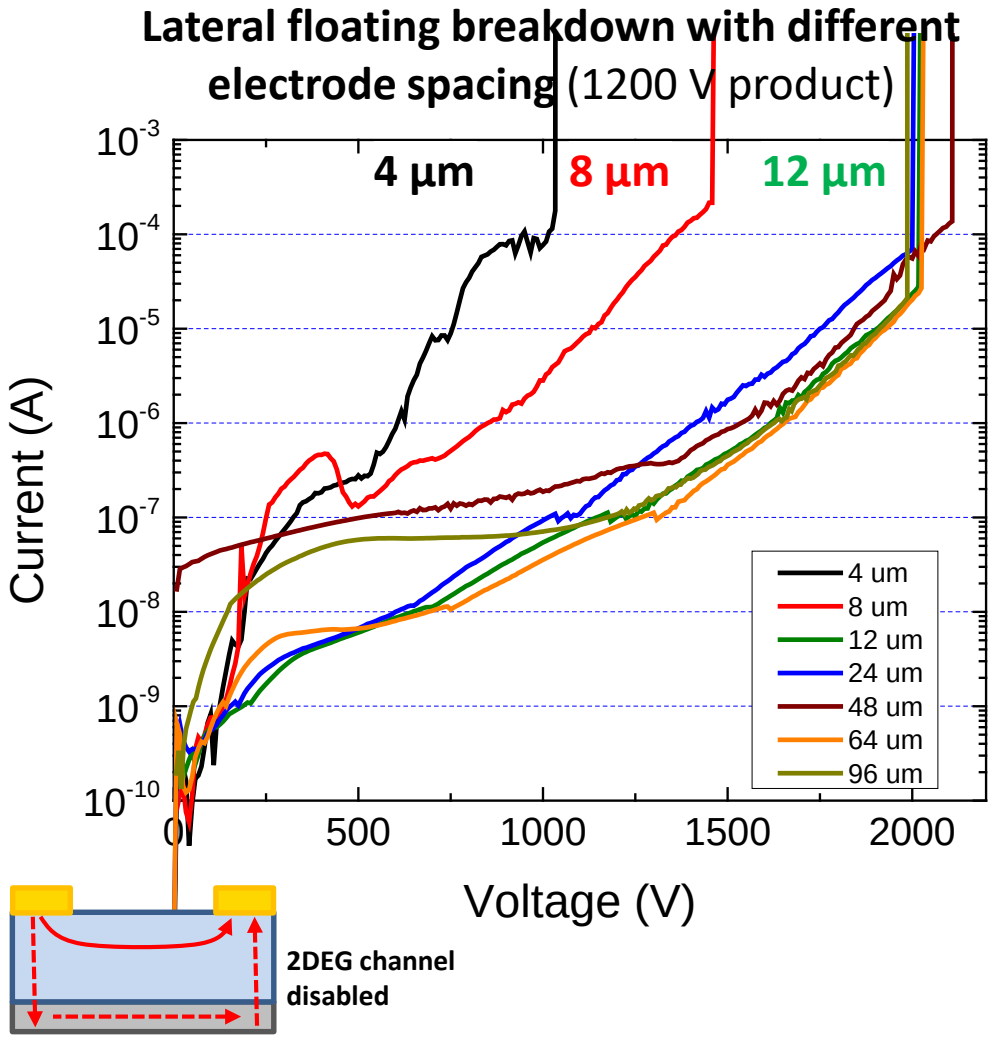
Vertical breakdown
(600 V and 1200 V products)

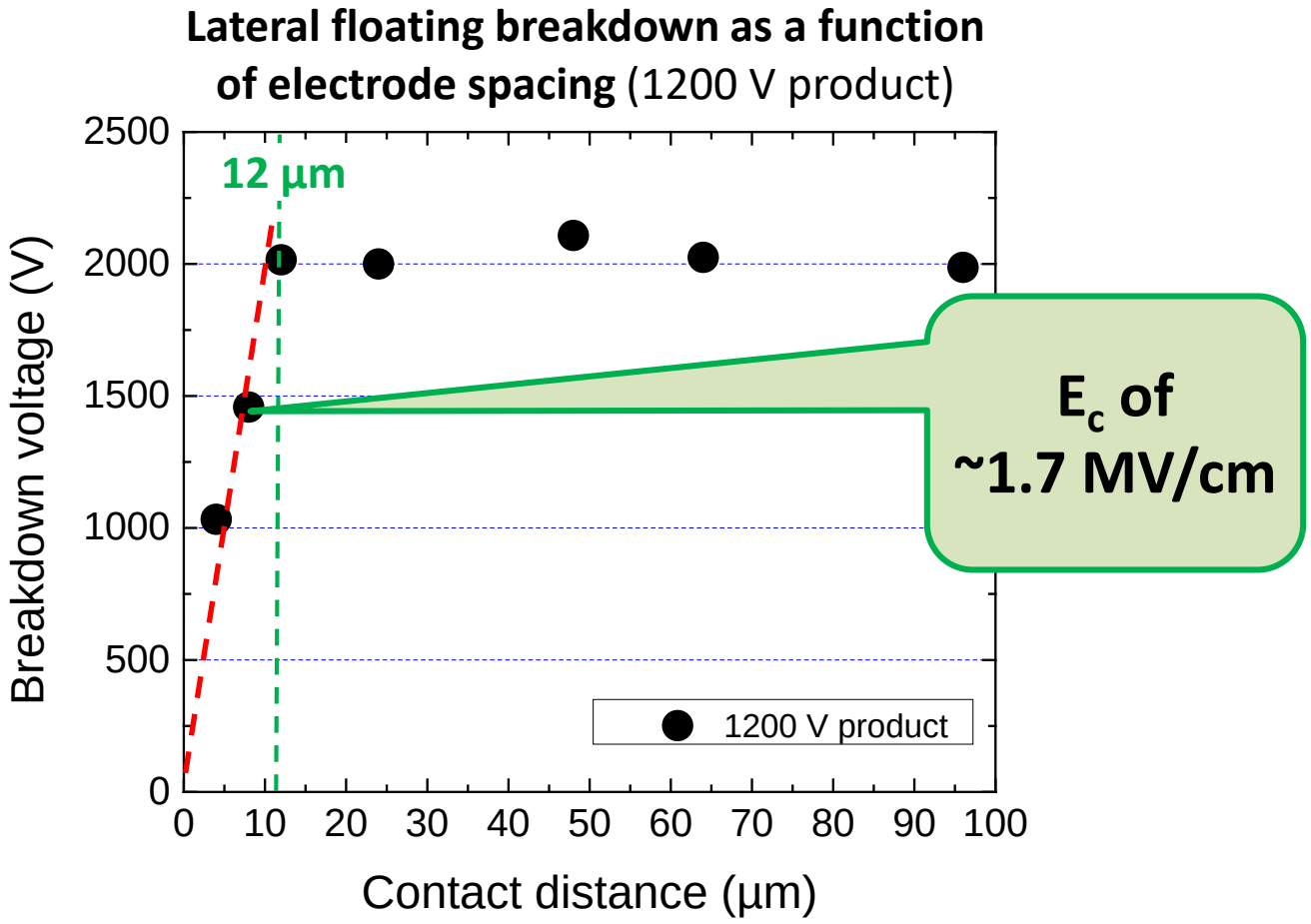


E_c of ~2.0 MV/cm

Data by courtesy of Dr. Farid Medjdoub and team at IEMN

The critical electric field is as high as 1.7 MV/cm for lateral, floating breakdown measurements

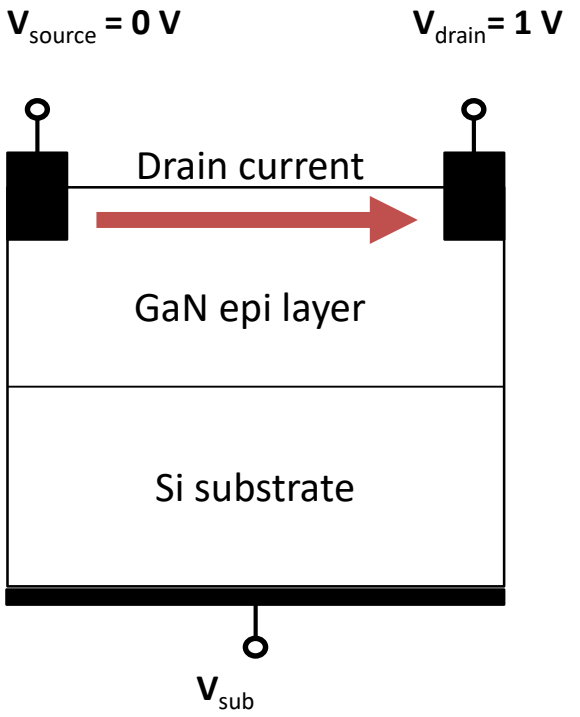




Data by courtesy of Dr. Farid Medjdoub and team at IEMN

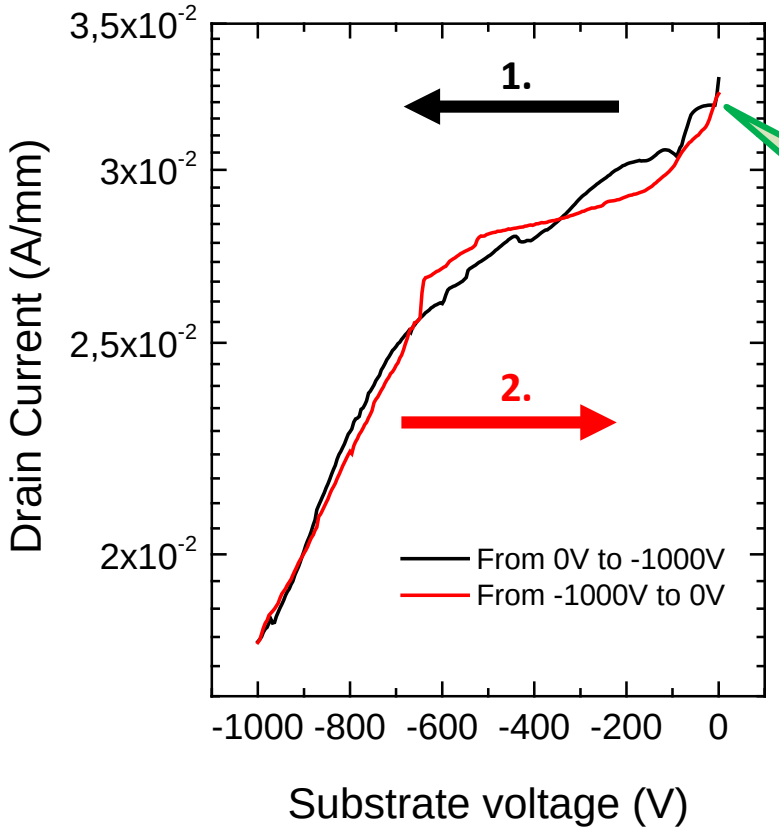
No hysteresis observed in back-gate bias sweeping measurement up to -1000 V, indicating low trapping effects in ALLOS' structure

Measurement setup
(room temperature)



Sweep from 0 to -1000 V and back to 0 V

Negative voltage ramp measurement
(ALLOS' 1200 V product)



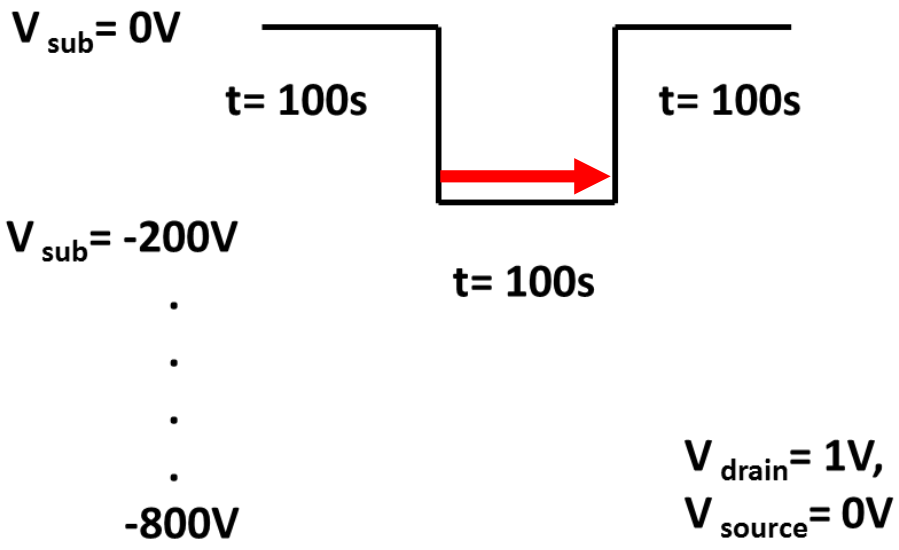
No hysteresis

Total sweeping time ~5 sec.

Graphs/data by courtesy of IEMN and University of Padova

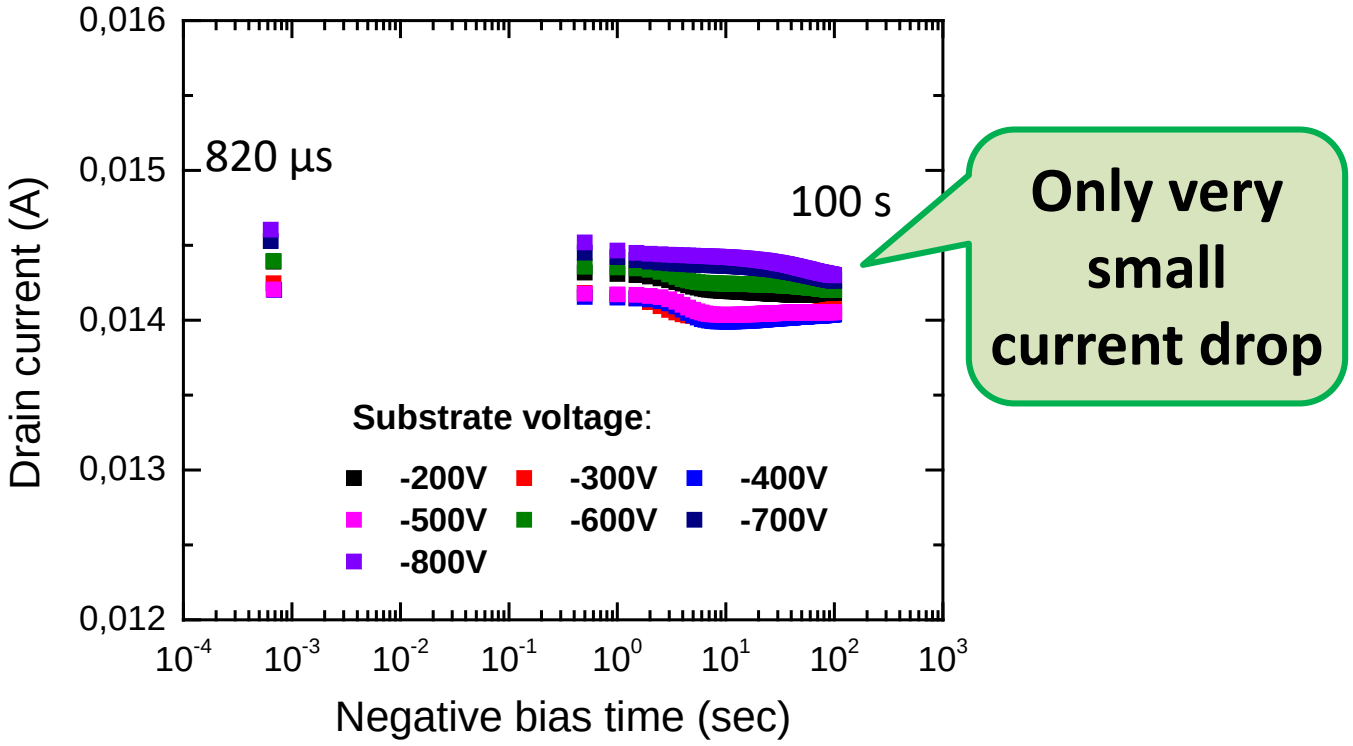
Back-gating transient measurements show very low trapping effects in ALLOS' GaN doping-free buffer with negative bias up to -800 V

Back-gating transient measurement setup



Drain current measured during negative bias up to -800 V

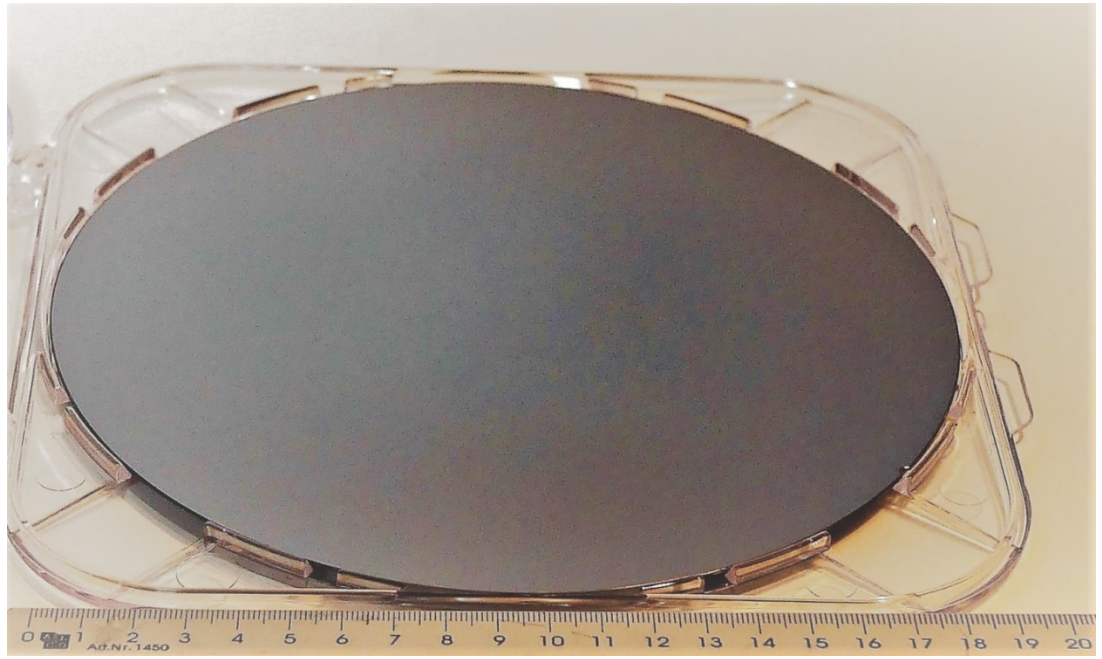
Back-gating transient measurement
(1200 V product, room temperature)



Graphs/data by courtesy of IEMN and University of Padova

This product prototype for 1200 V is based on ALLOS' established 600 V product and its superior quality and performance

ALLOS 200 mm GaN-on-Si epiwafer (600 V product)



Lowest possible residual strain

- ✓ 200 mm (725 µm thick) and 150 mm (625 µm)
- ✓ 7 µm thick with 0.3 % uniformity
- ✓ 30 µm bow, no cracks, thinning possible

Highest crystal quality

- ✓ XRD: 315 arcsec for (002), 415 arcsec for (102)
- ✓ TDD: $2x10^8$ cm^{-2}

Very low leakage currents and high breakdown voltage

- ✓ 0.003 µA/mm² vertical, 0.005 µA/mm lateral @ 600 V

Excellent Hall data

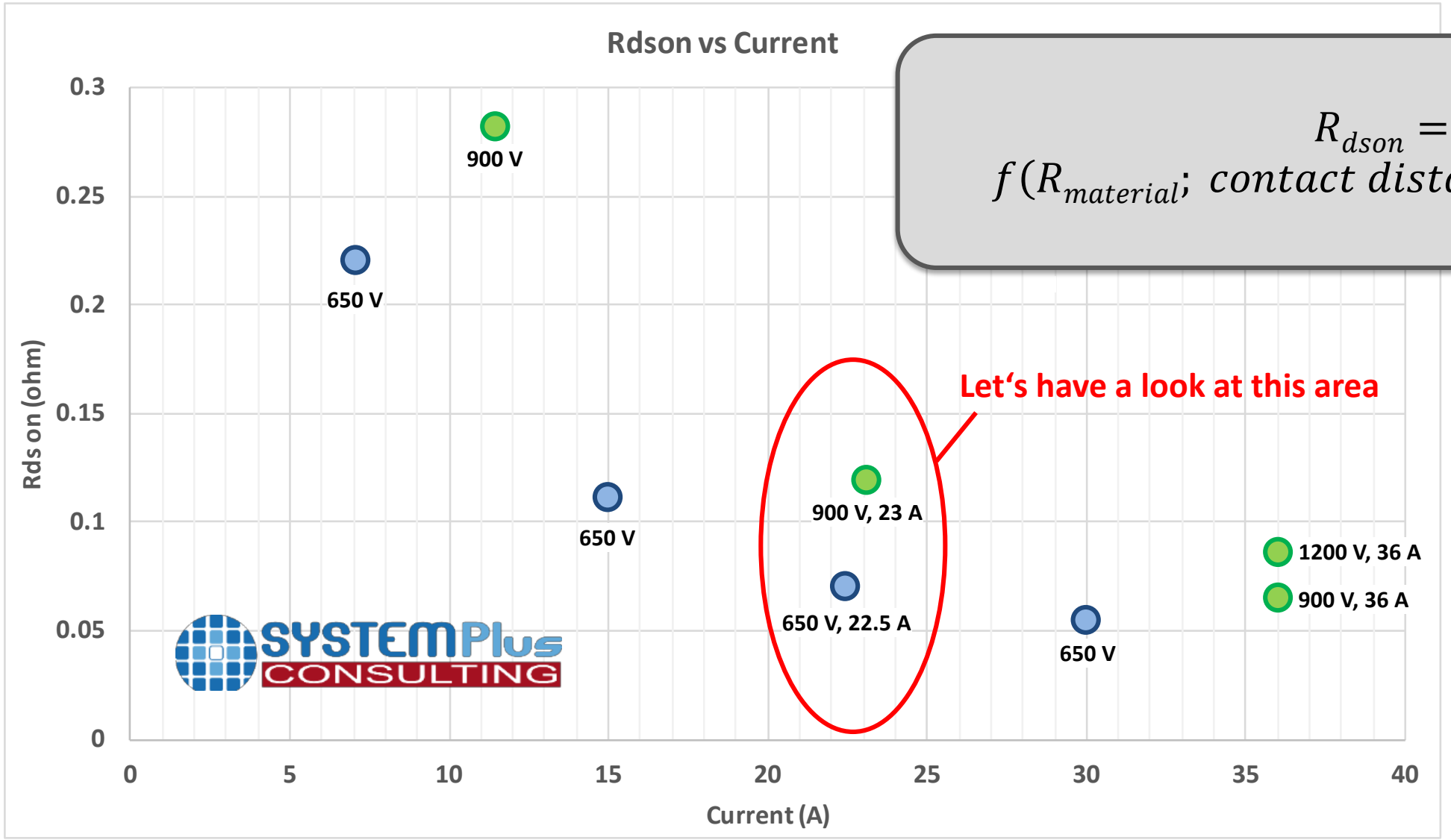
- ✓ R_{sheet}: 340 Ω/sq., Mobility ~2000 cm^2/Vs

A. Why is GaN-on-Si limited to 600 V today?

B. What can be achieved with ALLOS' technology?

C. Vision: How to attack SiC with 1200 Volt GaN-on-Si devices?

GaN can show its advantage in R_{dson} already today



$$R_{dson} = f(R_{material};\ contact\ distance;\ Rcontact)^*$$

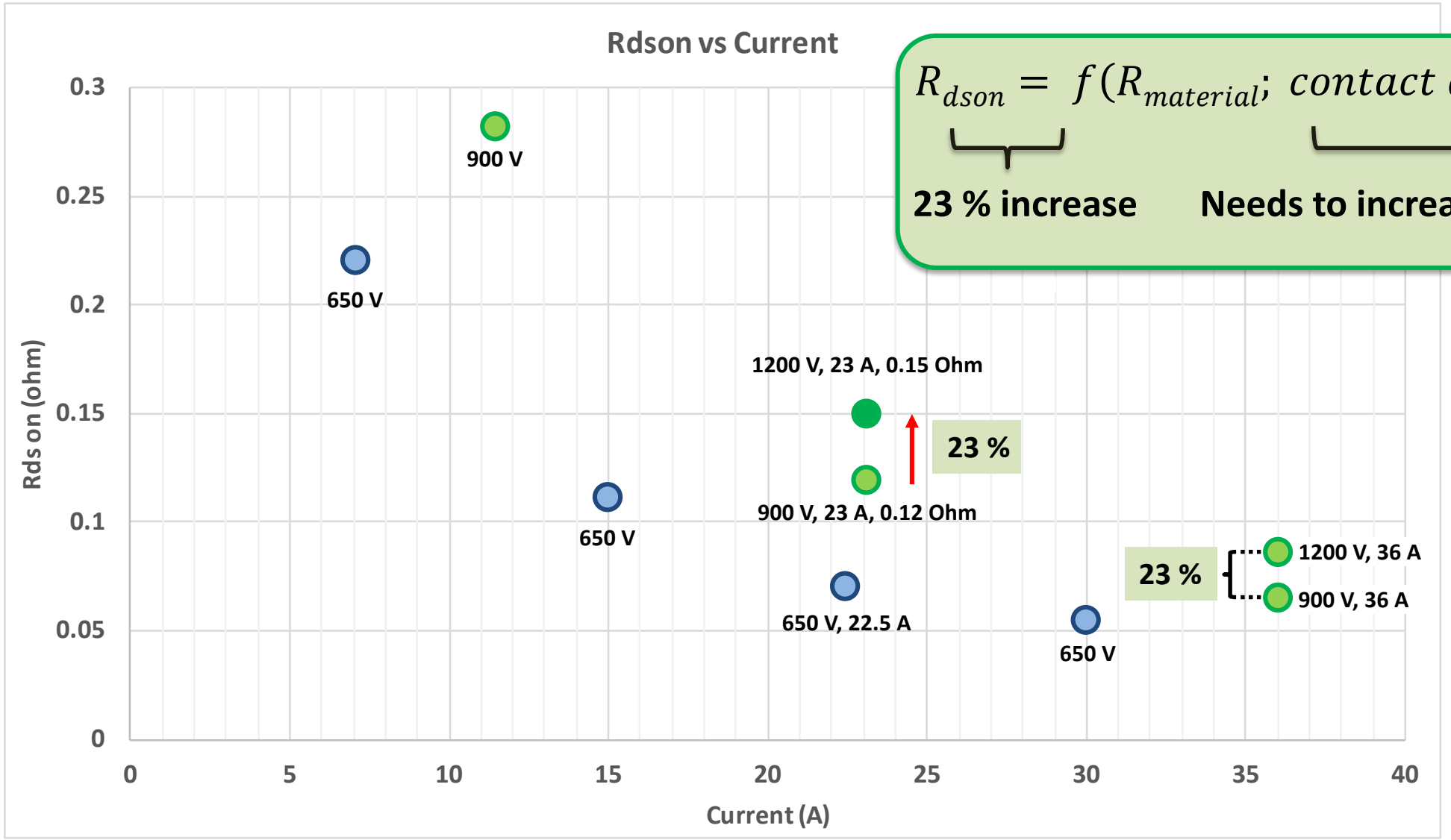
SYSTEMPlus CONSULTING

- Commercial SiC device vendor
- Commercial GaN-on-Si device vendor

* $R_{material}$ stands here for the resistance properties of the respective materials used. In GaN in particular sheet resistance R_{sheet}

In vertical devices „contact distance“ is also commonly known as „drift region“

Going to 1200 V increases R_{dson} for SiC by 23 %



$$R_{dson} = f(R_{material};\ contact\ distance;\ Rcontact)$$

23 % increase — **Needs to increase to sustain 1200 V**

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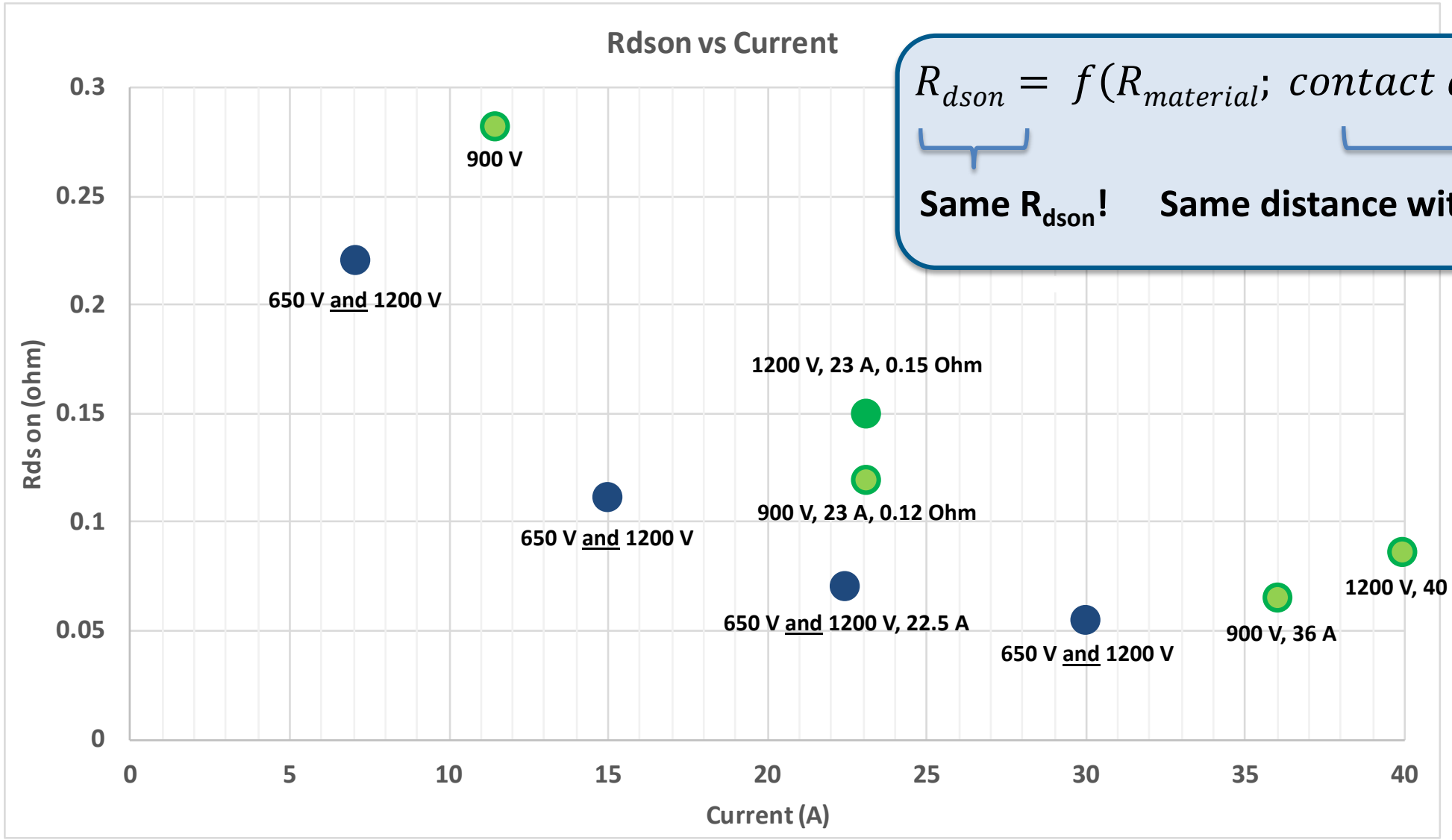
- Commercial GaN-on-Si device vendor

Estimate / projection:

- SiC 1200 V, 23 A, based on increase at 36 A

Moving to 1200 V with GaN does not increase R_{dson}



$$R_{dson} = f(R_{material};\ contact\ distance;\ Rcontact)$$

Same R_{dson}! **Same distance with ALLOS' GaN-on-Si**

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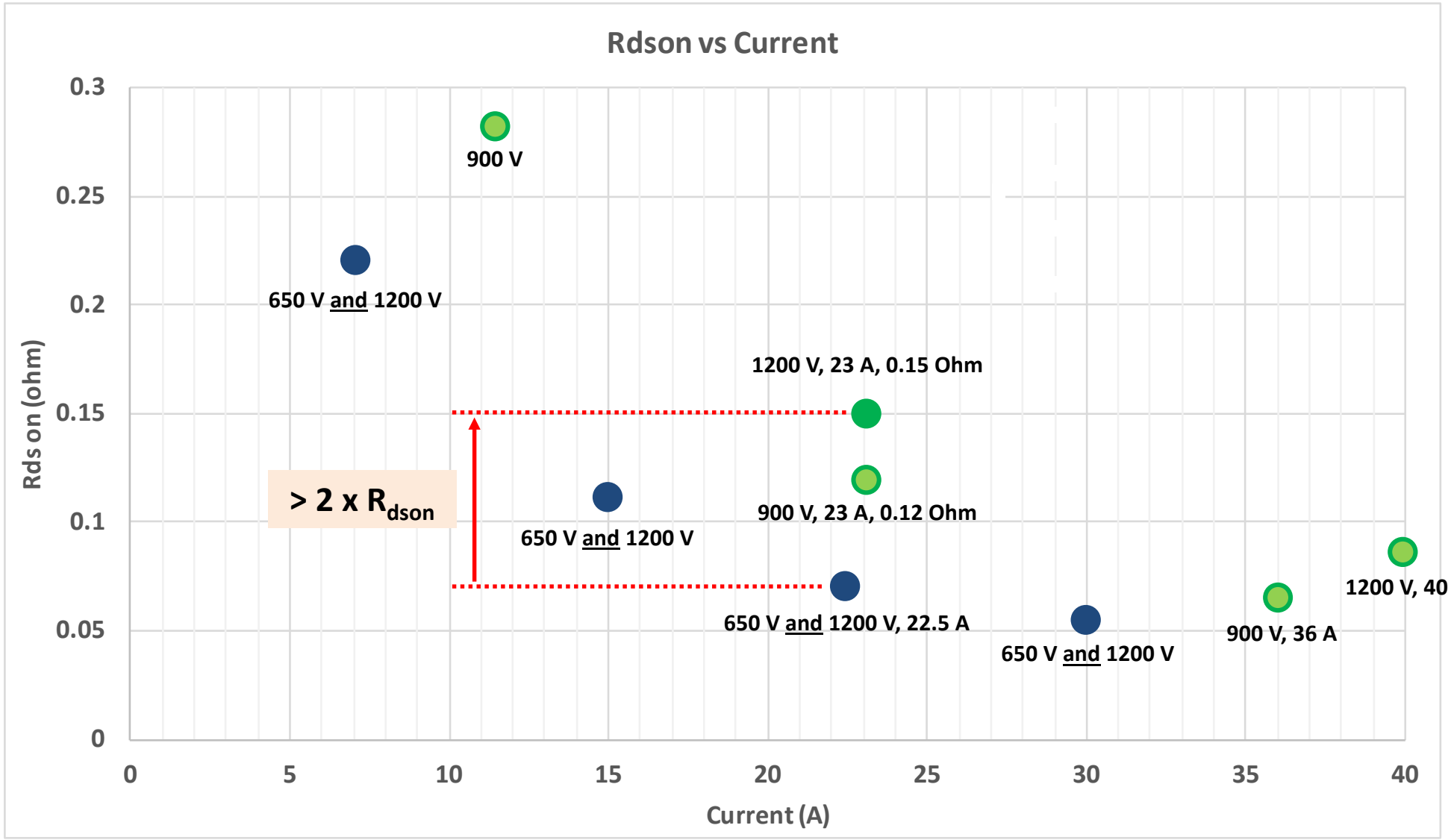
- Commercial SiC device vendor
- Commercial GaN-on-Si device vendor

Estimate / projection:

- SiC at 1200 V
- ALLOS GaN-on-Si at 1200 V

At 1200 V the SiC R_{dson} value is twice the GaN-on-Si R_{dson} value



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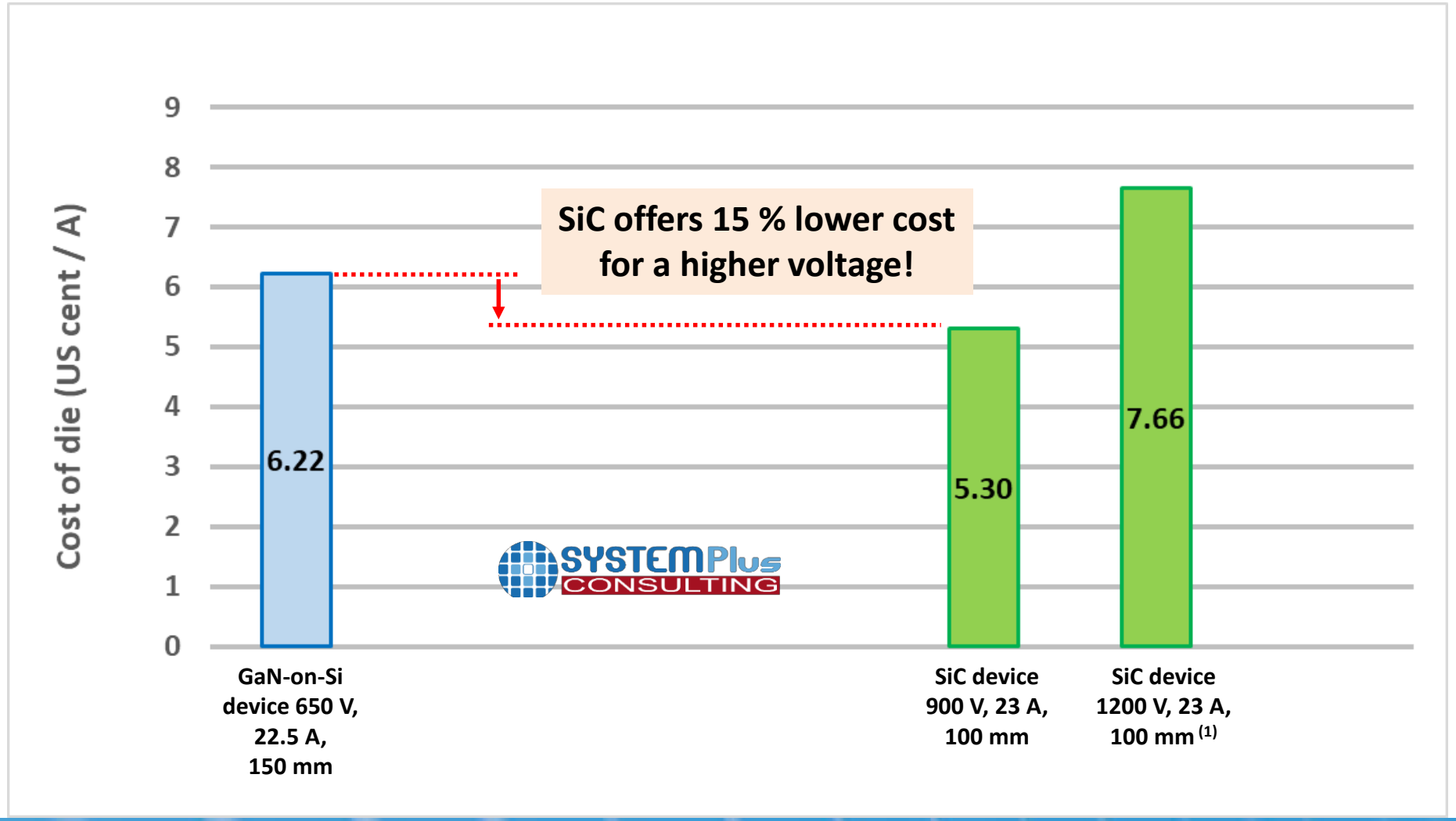
- Commercial GaN-on-Si device vendor

Estimate / projection:

- SiC at 1200 V
- ALLOS GaN-on-Si at 1200 V

The cost comparison shows a strong starting position for SiC



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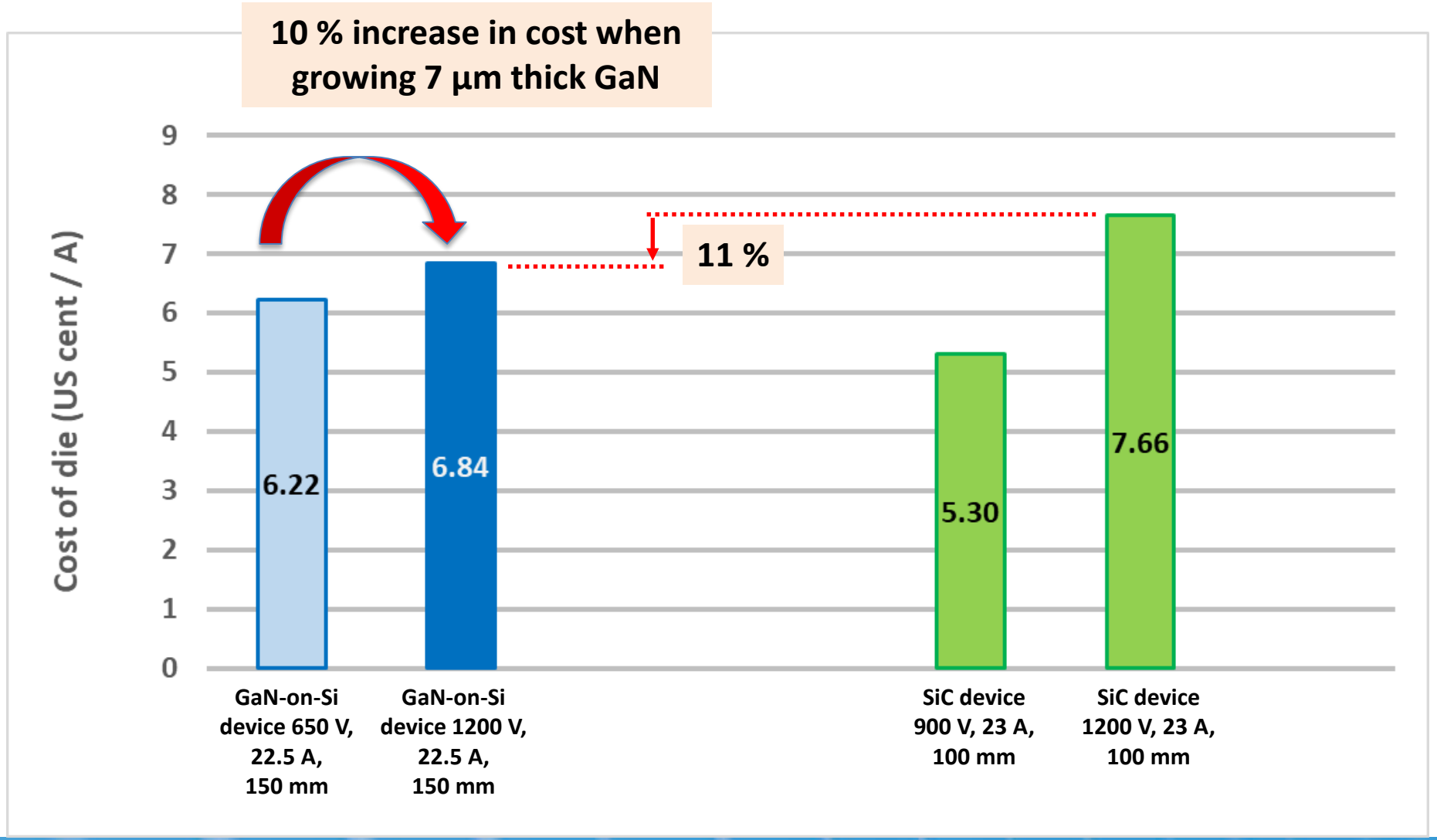
Commercial SiC device vendor

Commercial GaN-on-Si device vendor

(1) Estimate based on cost increase from 900 V to 1200 V for 36 A devices

At 1200 V GaN-on-Si gets a cost advantage



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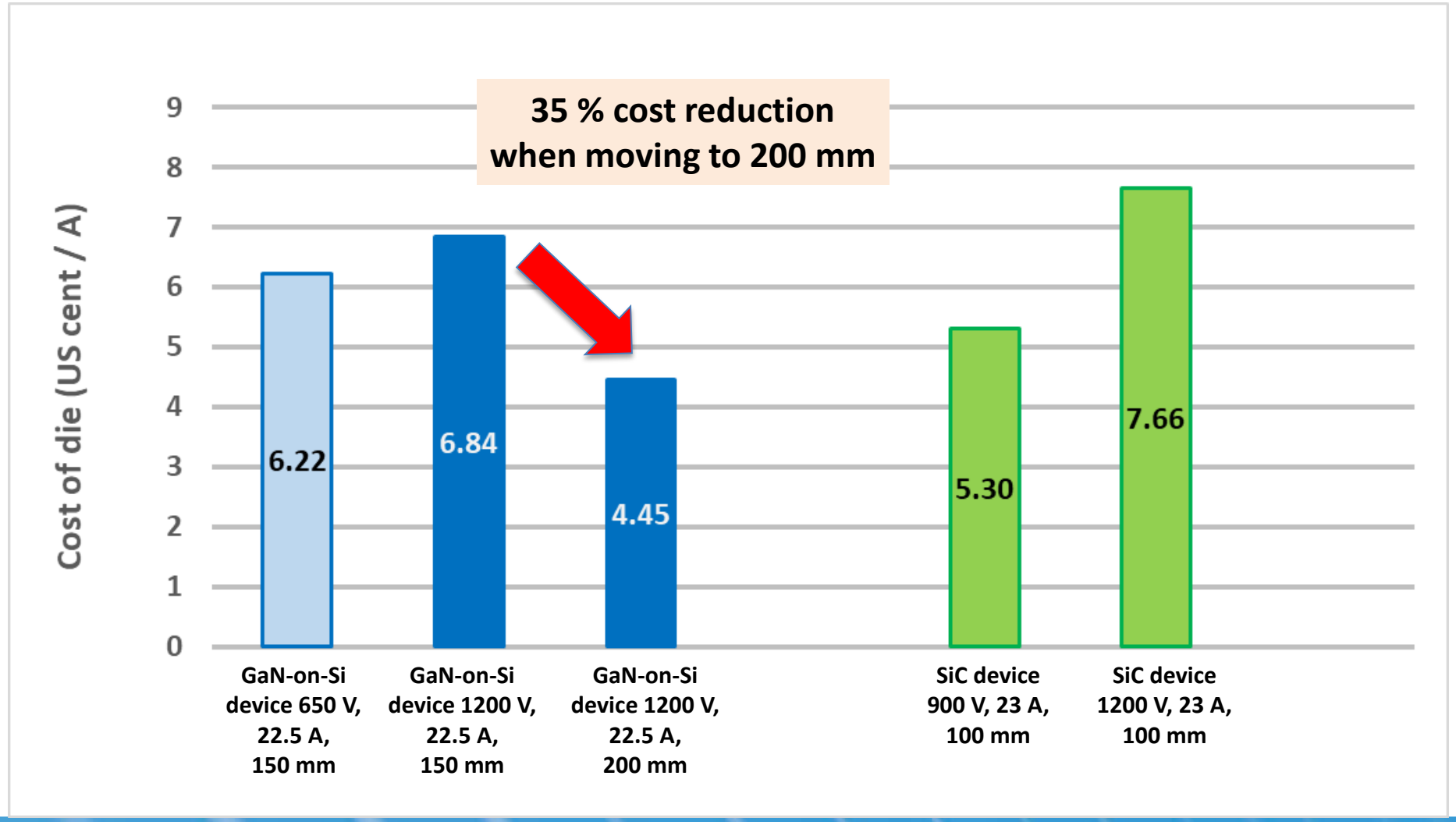
Commercial SiC device vendor

Commercial GaN-on-Si device vendor

Estimate / projection:

When using ALLOS' GaN-on-Si

ALLOS' GaN-on-Si can scale to 200 mm saving at least 35 % cost



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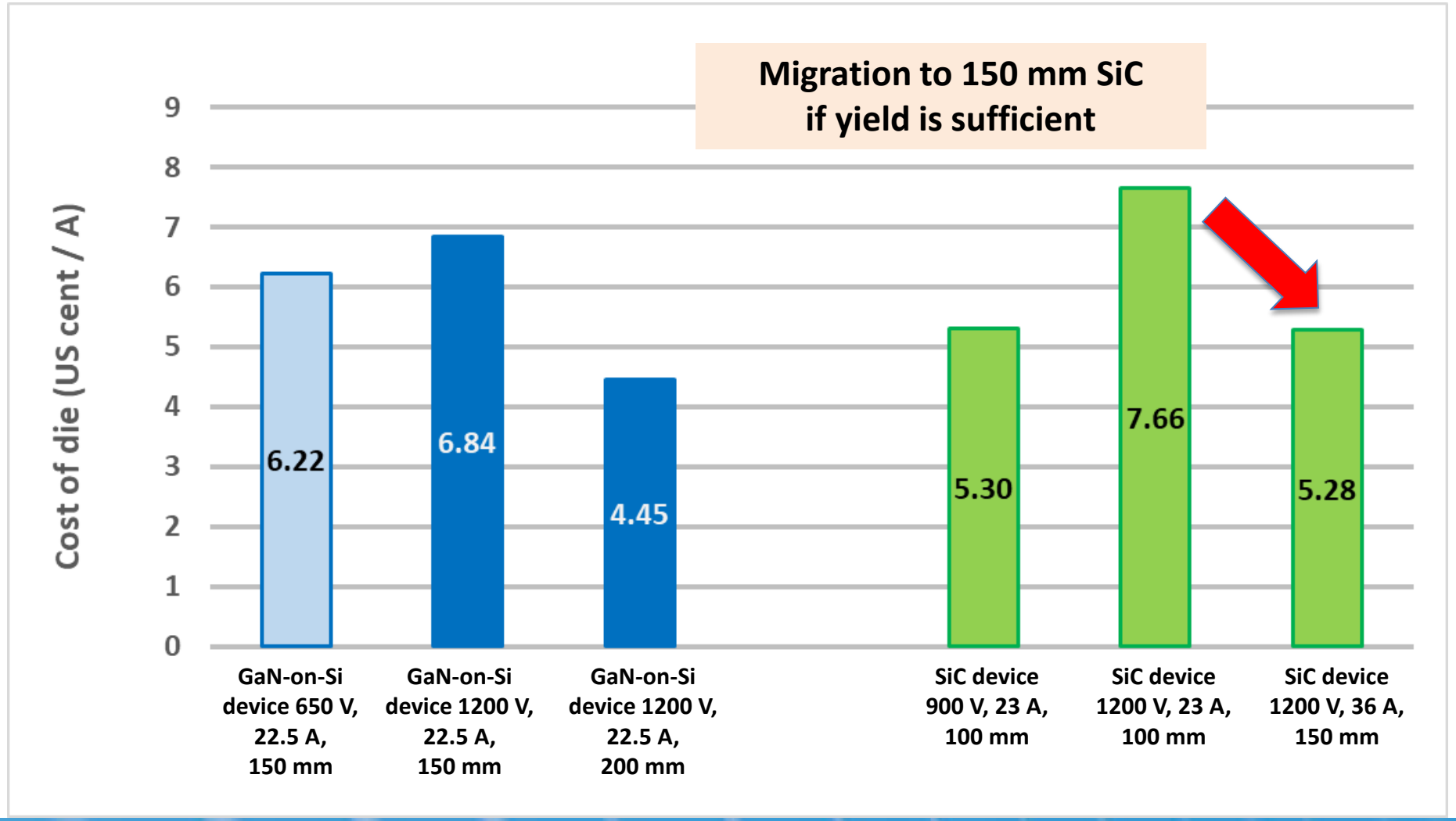
Commercial SiC device vendor

Commercial GaN-on-Si device vendor

Estimate / projection:

When using ALLOS' GaN-on-Si

SiC needs to solve its yield issues at 150 mm to reduce cost



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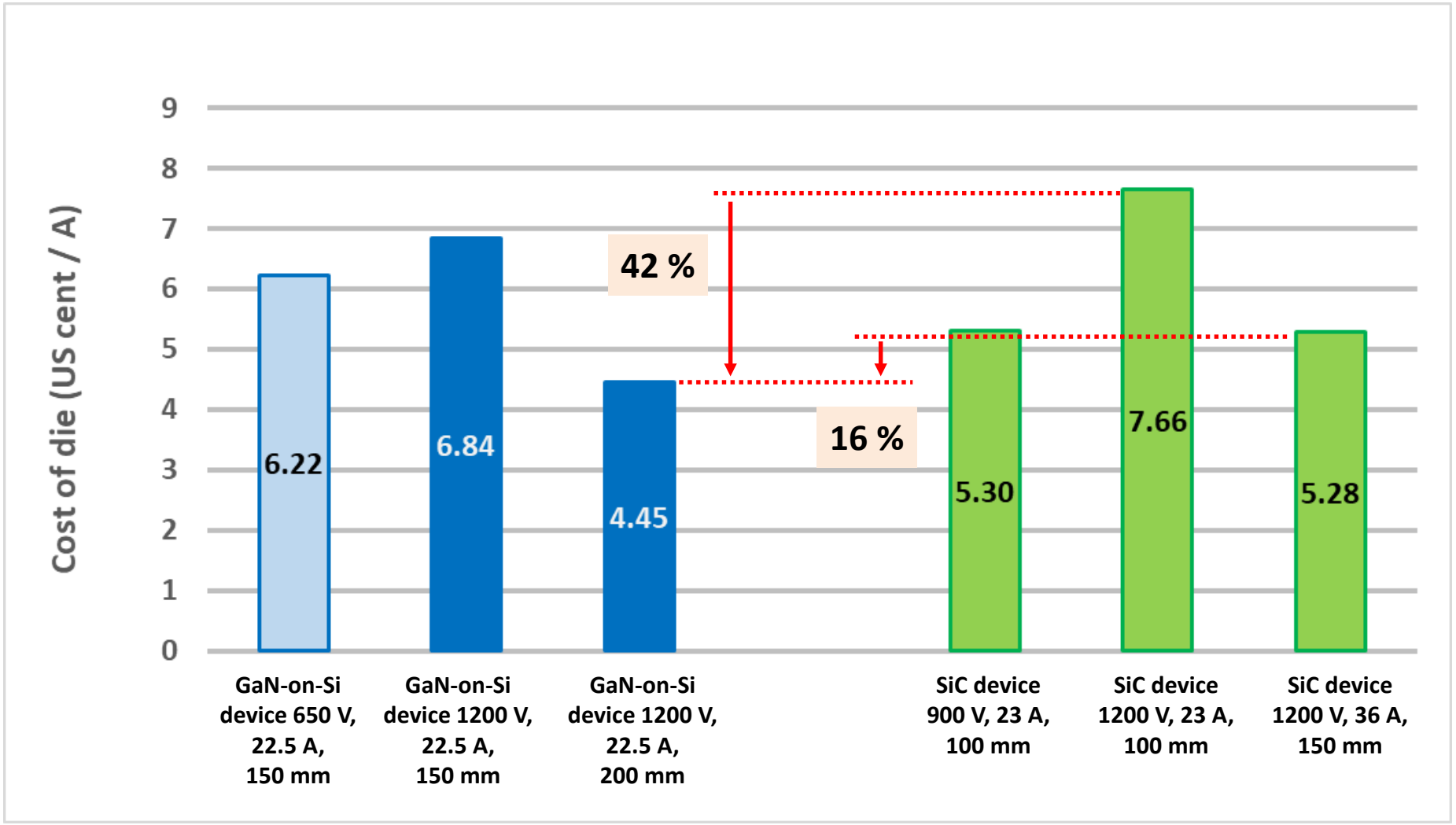
Commercial SiC device vendor

Commercial GaN-on-Si device vendor

Estimate / projection:

When using ALLOS' GaN-on-Si

At 1200 V ALLOS' technology on 200 mm enables a cost advantage



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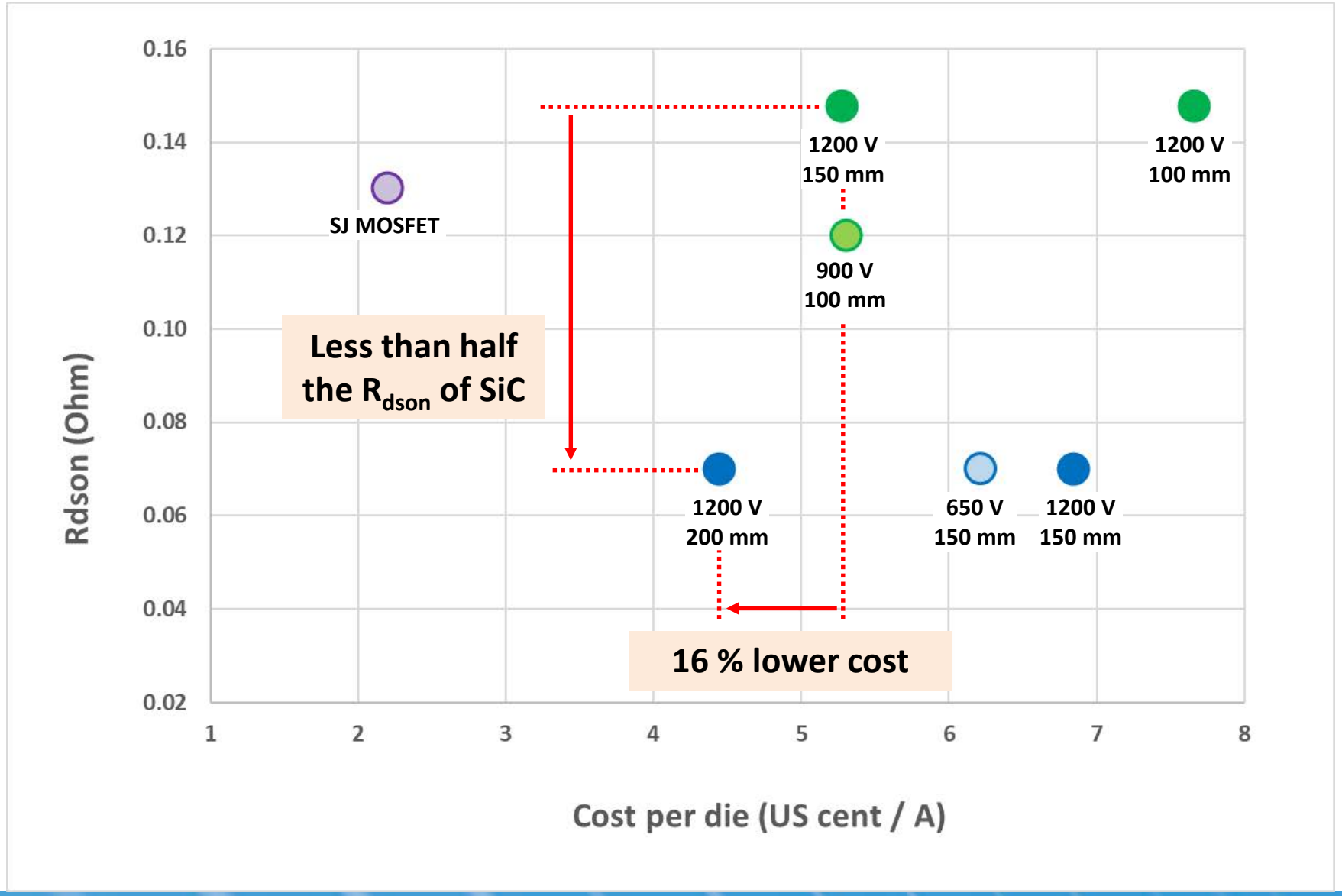
Commercial SiC device vendor

Commercial GaN-on-Si device vendor

Estimate / projection:

When using ALLOS' GaN-on-Si

Summary: 1200 V GaN-on-Si can attack SiC on performance and price



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- Commercial SiC device
- Commercial GaN-on-Si device
- SJ MOSFET benchmark

Estimate / projection:

- SiC at 1200 V
- When using ALLOS' GaN-on-Si

Conclusion and outlook

ALLOS' GaN-on-Si is the right basis to advance into SiC territory

1. A Vbr of 1400 V vertical and lateral is achieved
2. Indications for very low trapping effects
3. The existing R_{dson} advantage of GaN-on-Si over SiC is expected to widen further when moving to 1200 V devices
4. 200 mm wafer for 1200 V provide a cost advantage over SiC 100 and 150 mm

ALLOS seeks a partner to develop and commercialize this technology

- Accelerating existing epi development program
- Working for device vendors to combine the strengths of this material and advanced device technology
- Identify and target attractive applications above 650 V

Thank you for nominating us!

Thank you

for voting for us!

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