ALLOS Semiconductors

Silicon or sapphire

Which substrate will meet the yield and cost requirements for micro LED displays?

2020 World Display Industry Conference, 21st November 2020,
online meeting, presented by Alexander Loesing, co-founder of ALLOS

Outline

1. Introduction to ALLOS
2. Silicon or sapphire for mass production of micro LED
3. ALLOS' 1 bin® LED epiwafer technology for high yield and cost-competitive mass production
4. Conclusion

ALLOS* is a leader in GaN-on-Si with 17 years successful track-record

end of 90s — University of Magdeburg one of three birthplaces of GaN-on-Si world-wide

2003 — AZZURRO founded in Magdeburg and becomes the first epiwafer vendor world-wide

2005 — First to show a 150 mm epiwafer

2005 — Products for HPE, RF and LED introduced

2009 — OSRAM gets license for LED production

2009 — First to offer a commercial 200 mm epiwafer

2013 — AZZURRO closes

2013 — ALLOS buys IP and technology for new business model

2013 — Total investment exceeds EUR 40 m

2014 — Carbon-doping free GaN-on-Si

2015 — EPISTAR licenses ALLOS' technology

2016 — ALLOS shows < 1 nm wavelength uniformity on 200 mm GaN-on-Si LED epiwafer on Veeco Propel

2016 — For > 1400 V breakdown

2018 — IEMN: "Excellent trapping behavior"

2019 — ALLOS sold its electronics business and focuses purely on micro LED

2020 — Overcome trade-off between leakage and switching

* ALLOS and predecessor company AZZURRO

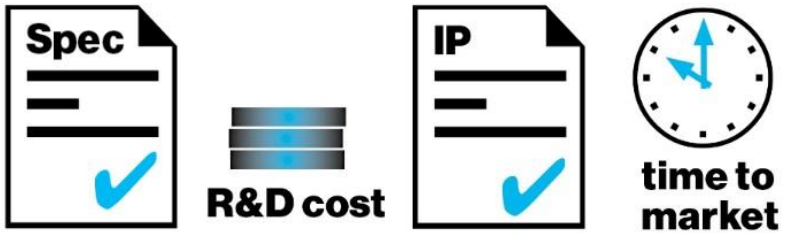
ALLOS' value proposition is to license and transfer turn-key GaN-on-Si epiwafer technology and IP

3 years ?

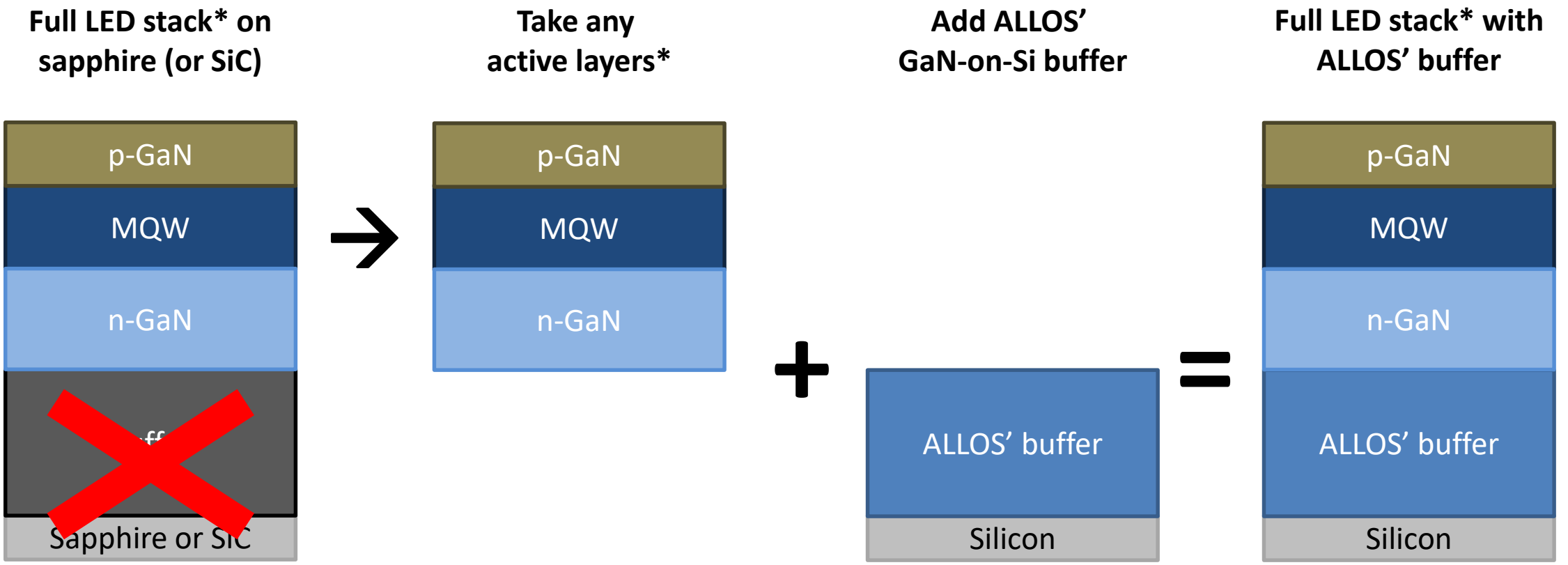
Develop GaN-on-Si epitaxy technology by yourself

Work with ALLOS

12 weeks



With only few runs any active layers can be integrated on ALLOS' buffer – also all colors: Blue / green / red



* This can be from ALLOS' customer or a third party (e.g. by licensing the LED stack)

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Silicon or sapphire? Why ask this question?

- ✓ GaN-on-sapphire is the material of choice for (conventional) LEDs
- ✓ Most micro LED displays demonstrated today use GaN-on-sapphire

BUT

Micro LEDs are much smaller and thus more difficult to make

Monolithically integrated displays need diameter to match CMOS

Required yield levels make quantum leap of yield necessary

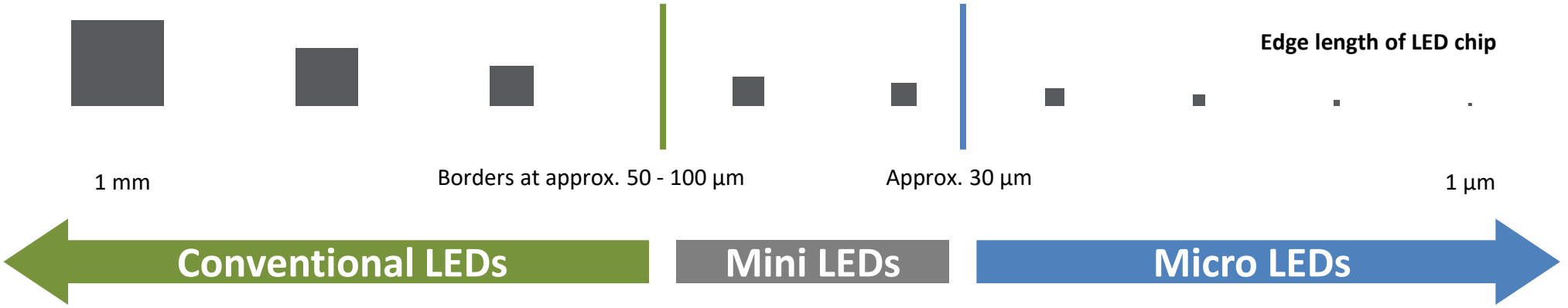
Micro LEDs require thin-film designs (substrate removal)

'Square packing' becomes a crucial cost driver

Cost is hugely driven by yield in processing steps after epi

Micro LEDs are much smaller and thus more difficult to make

What is the difficulty of working with micro LEDs?



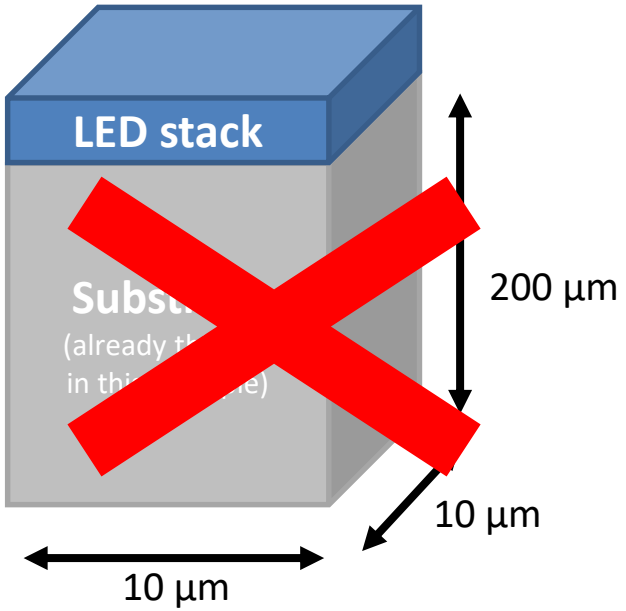
- ➔ Micro LEDs are super tiny (and thinner) and difficult to handle
- ➔ The much smaller size requires improved processing skills, cleanroom and sophisticated silicon industry level processing tools
- ➔ The amount of chips *explodes*: On a single 200 mm micro LED wafer you have > 600 million micro LED chips of 5 x 5 µm² which requires new approaches

Micro LEDs require thin-film designs (substrate removal)

GaN-on-Si enables low cost & high yield thin-film LEDs

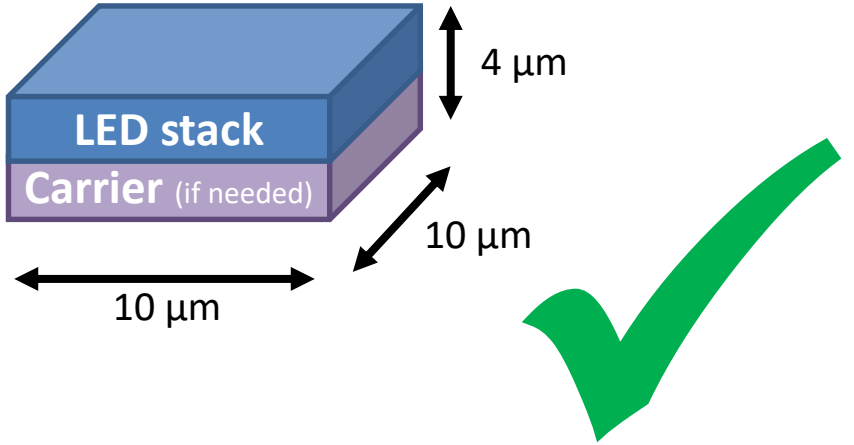
Lateral or flip-chip LED*

Does not work for micro LED



- → **With conventional chip designs it is difficult and costly to achieve the desired thinness**
- → **The aspect ratio makes use of thin-film LED chips necessary for micro LEDs**

Vertical or thin-film (flip-chip) LED*



- → **Laser-lift-off on sapphire will not achieve the required yield, in particular on ≥ 200 mm**
- → **Bonding ALLOS' GaN-on-Si epiwafers is easier because of low, precisely controlled bow**
- → **Vertical and TFFC designs favor use of silicon for easier substrate removal with high yield**

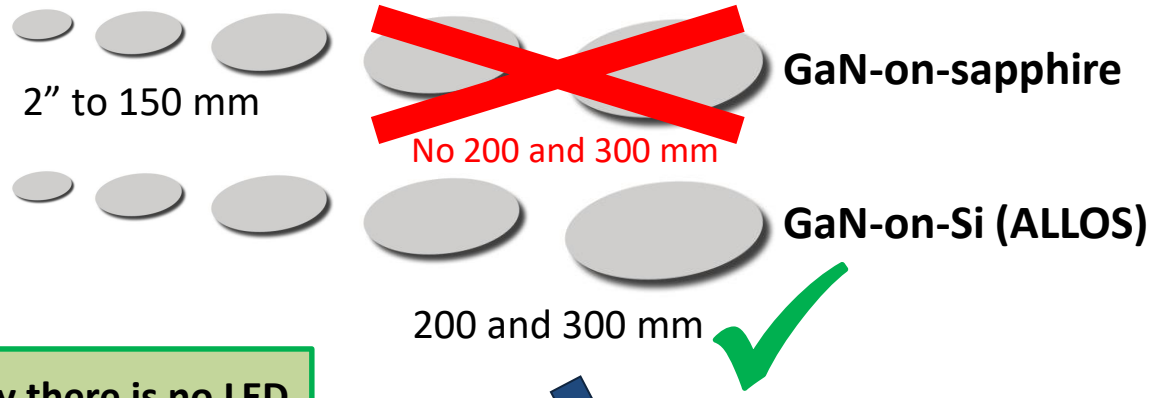
* Drawings not to scale and dimensions are examples of possible micro LED chips (thin-film vertical or thin-film flip-chip [TFFC])

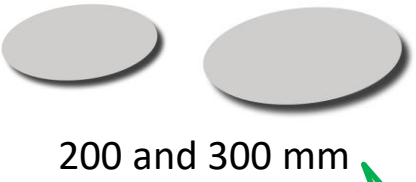
Monolithically integrated displays need diameter to match CMOS

Augmented reality (AR) displays require CMOS driver

LED epiwafer growth and micro LED processing

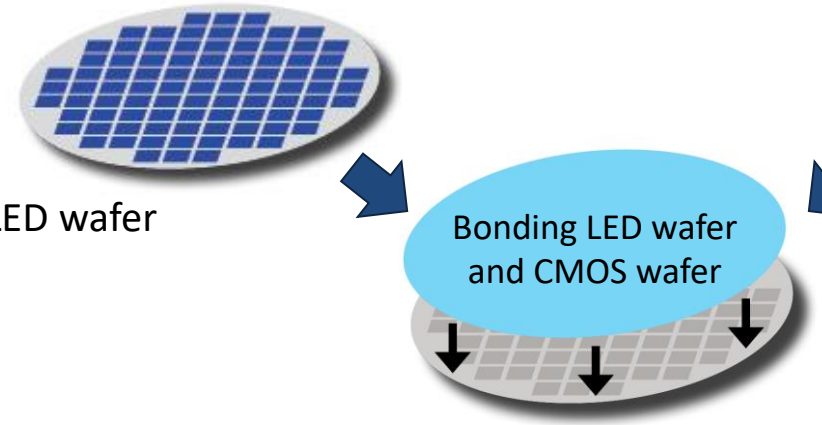
CMOS driver / backplane





Today there is no LED processing line capable of 200 and 300 mm processing

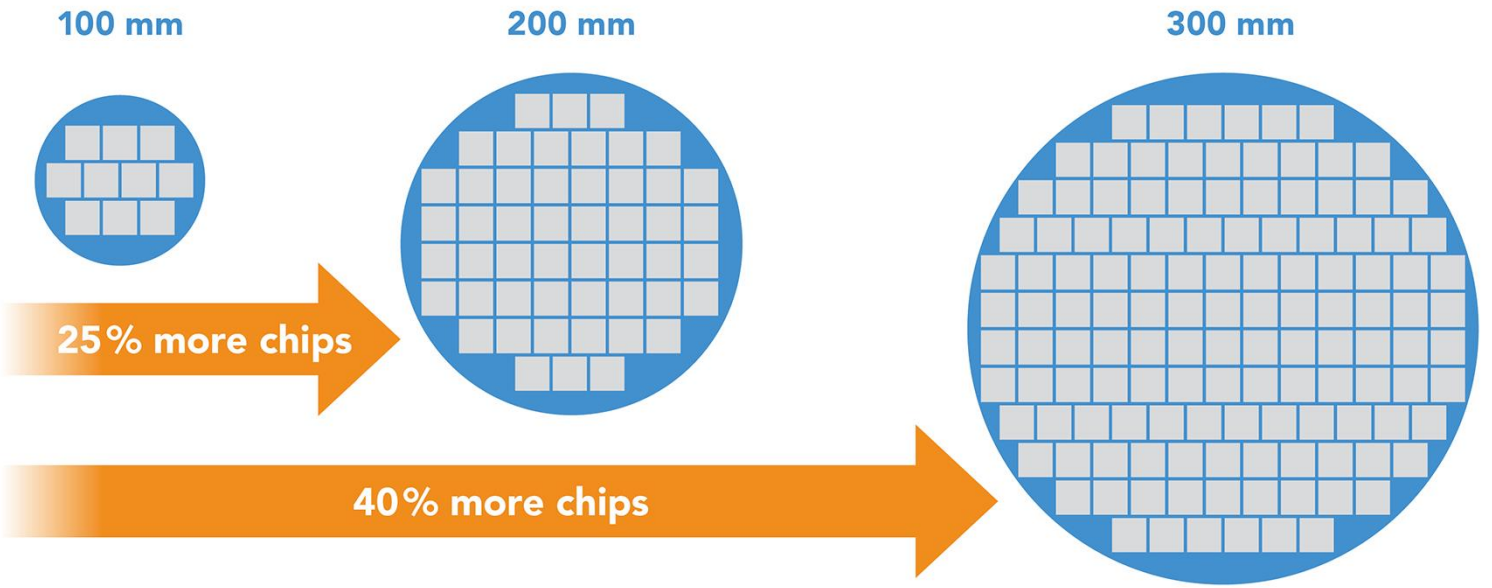
The required yield and precision levels make use of silicon industry standards necessary



Strong push to 300 mm for higher energy efficiency and functionality

'Square packing' becomes a crucial cost driver

Better area utilization enables LED chip cost reduction



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= Transfer stamp size (example)

Wafer size [in mm]	Wafer area [factor]	Amount of stamps	Cost advantage
100	1	10	NA
200	> 4	50	> 25 %
300	> 9	128	> 40 %

- Efficient micro LED manufacturing requires usage of a transfer stamp
- Higher transfer efficiency with larger transfer stamp
- Useable area for given transfer stamp is larger with bigger wafers

This is in addition to all other advantages coming from using larger wafers

Likewise you have the cost advantage also for AR displays by getting more displays per area

Required yield levels make quantum leap of yield necessary

The yield challenge in numbers…

- **A standard 4K UHD display has 3,840 x 2,160 pixels (= 8,294,400)**
- **For an RGB display you thus need more than 24,800,000 micro LED chips**

Relevant yield*	… equals amount of chips failing
90.00000 %	2,488,320.00
95.00000 %	1,244,160.00
99.00000 %	248,832.00
99.90000 %	24,883.20
99.99000 %	2,488.32
99.99900 %	248.83
99.99990 %	24.88
99.99999 %	2.49

Even a **Six Sigma** = 99.99 % defect-free process will require 2,488 chips to be repaired on a 4K UHD display

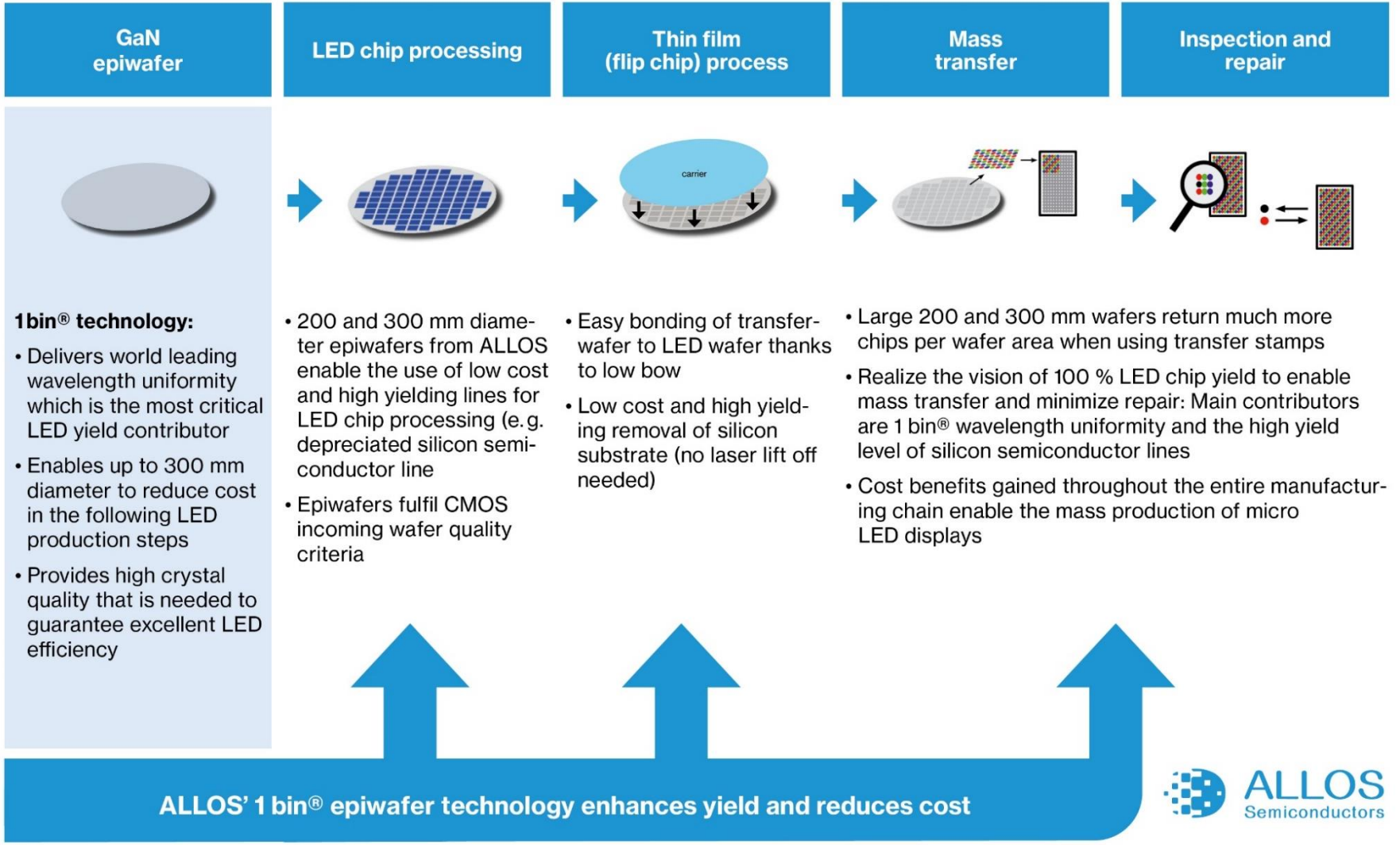
→ Uniformity of epiwafers needs to be improved drastically

→ It becomes essential to use the high yield of silicon processing lines

* Combined yield of all processes including on-wafer yield, LED chip making yield, transfer yield, etc.

Cost is hugely driven by yield in processing steps after epi

Uniform epiwafers improve the cost and yield of the entire production chain



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Essential requirements for micro LED achieved by ALLOS

High crystal quality

- ✓ Same low defect level as on GaN-on-sapphire: TDD ~2 x 10^8 cm^{-2}

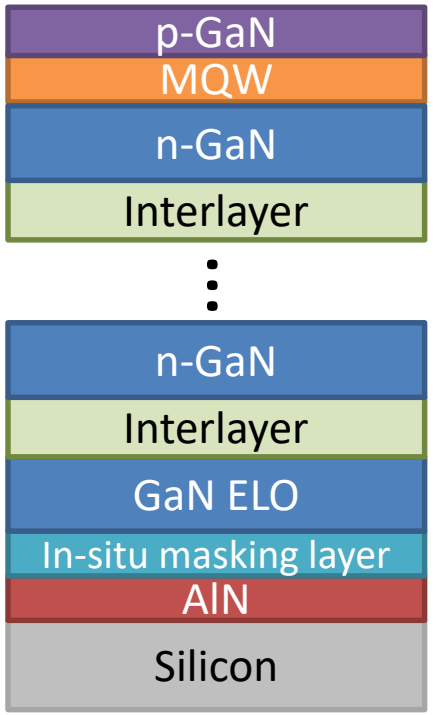
= Performance

Large diameter and CMOS ready

- ✓ 200 mm and 300 mm diameter
- ✓ < 30 µm bow for 725 µm (200 mm) and 775 µm (300 mm) thickness
- ✓ No cracks, no residual strain

= Low-cost

Typical GaN-on-Si LED structure of ALLOS*



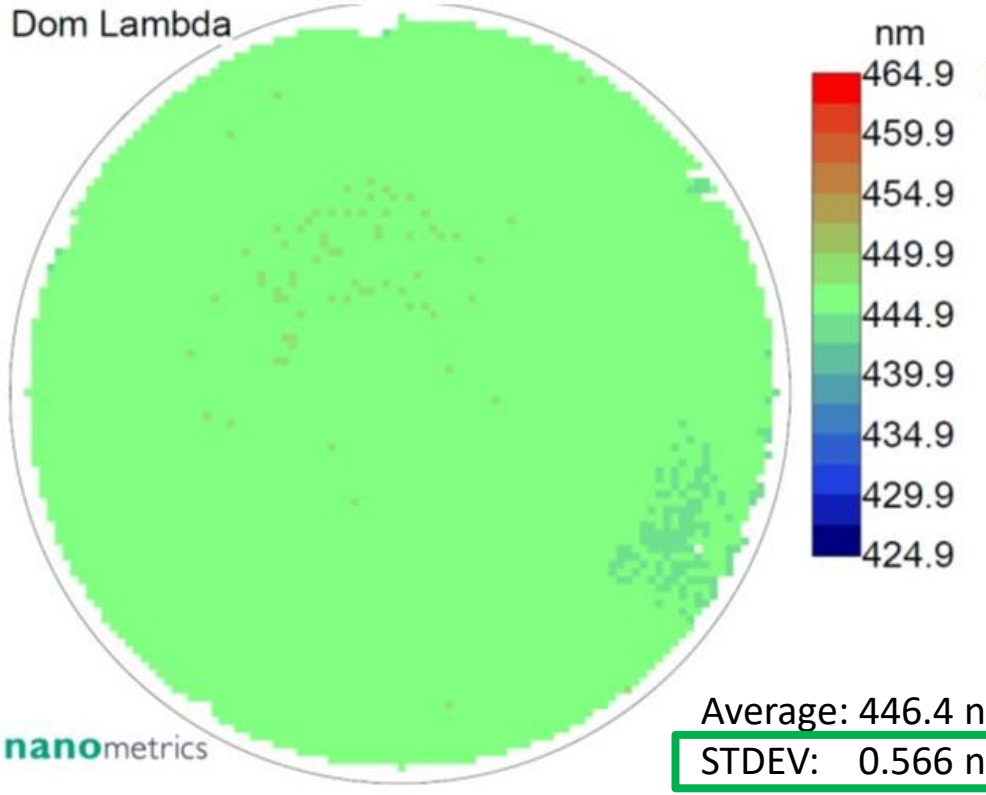
Excellent wavelength uniformity

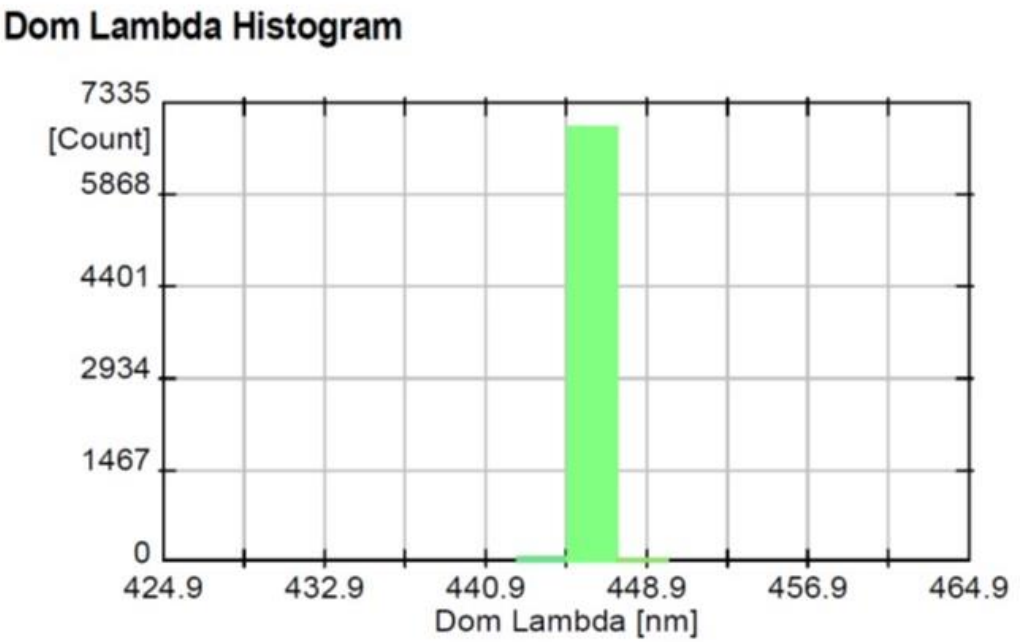
- ✓ Requires perfect conditions for MQW growth…
- ✓ … which cannot be achieved on sapphire - especially not at similar wafer diameters…
- ✓ … and needs to be repeatable

= High yield

*** Protected by ALLOS' IP; active layers can be the same structure as used by customer for GaN-on-sapphire**

Record-breaking emission uniformity < 0.6 nm is achieved on 200 mm GaN-on-Si micro LED epiwafer



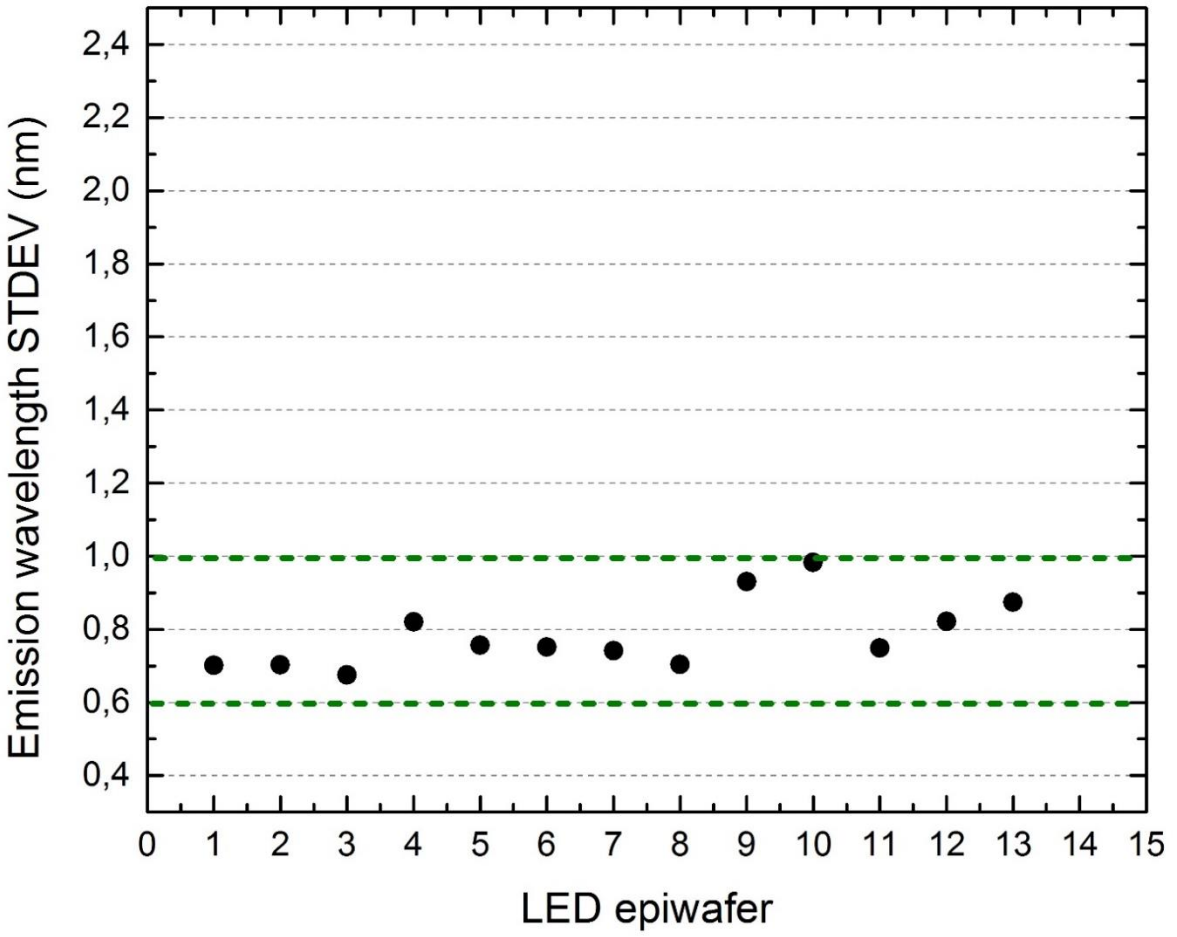


Average: 446.4 nm
STDEV: 0.566 nm (0.127 %)
Median: 446.4 nm
Min: 444.6 nm
Max: 447.9 nm

97.6 % in 2.5 nm bin
Min-max = +/- 1.65 nm

Result from customer project on Veeco Propel in February 2019

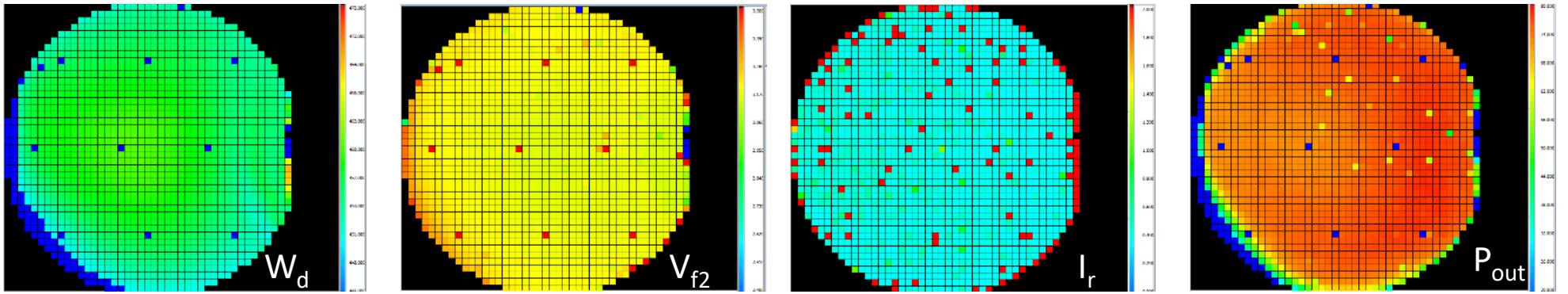
Excellent reproducibility for emission wavelength uniformity



13 repetition runs with average STDEV of wavelength uniformity of 0.79 nm and all points below 1 nm (STDEV of average value is 0.095 nm)

Result from customer project using the same recipe on Veeco Propel in January 2020

Low V_f and high P_{out} are on a par with GaN-on-sapphire LEDs

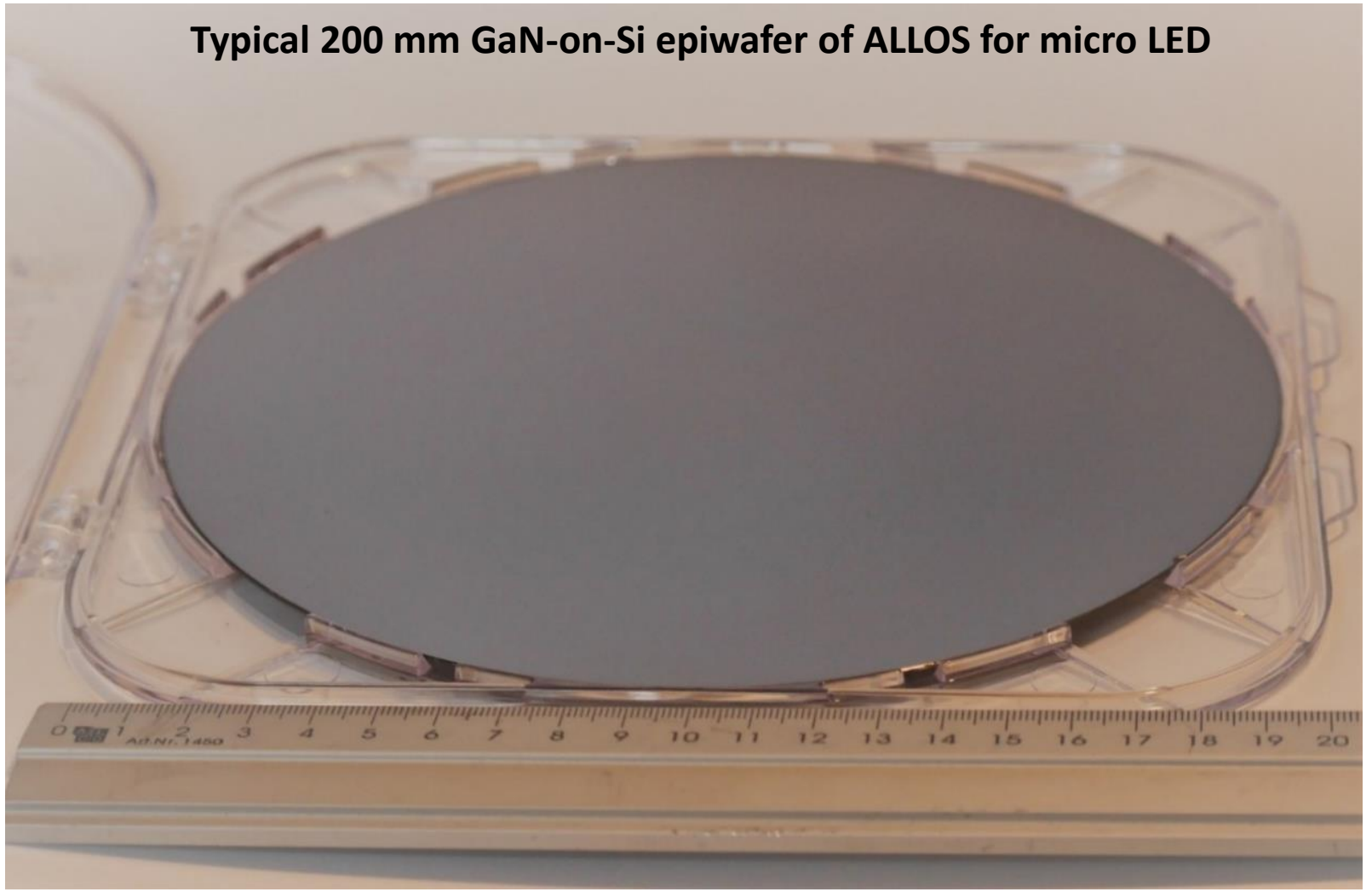


@ 350 mA	V_{f1} (@10 µA)	V_{f2} (Volt)	V_r (Volt)	I_r (µA)	P_{out} (a. u.)	W_d (nm)	P_{out} to mass production GaN-on-sapphire LED
GaN-on-Si LED	2.21	3.12	15.24	0.06	69.0	451.7	97 %

Result from customer project on Veeco K465i already in 2015, using customer's mass-production GaN-on-sapphire LED structure on ALLOS' GaN-on-Si buffer

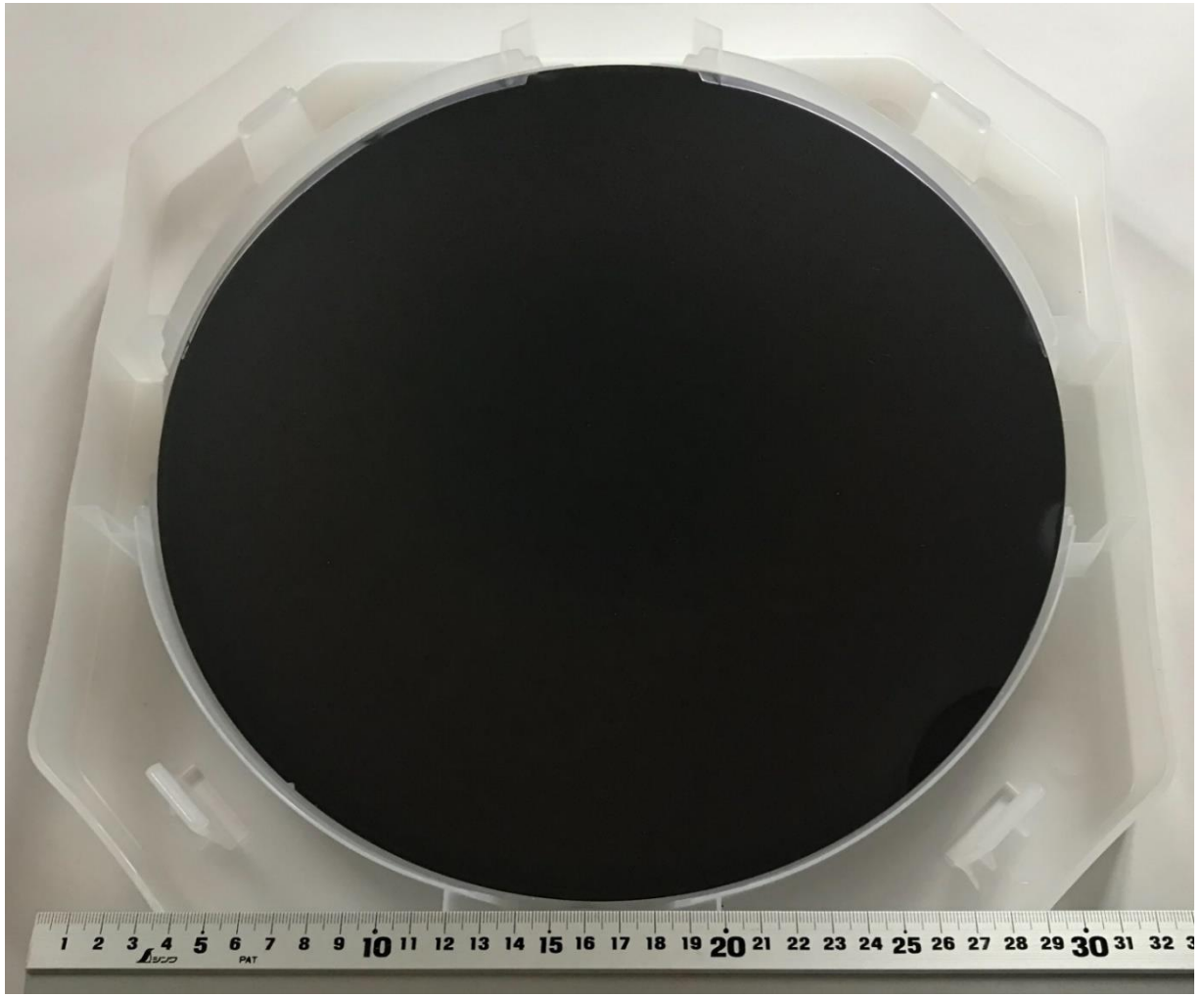
ALLOS‘ GaN-on-Si epiwafer technology is the key enabler for 1 bin® low-cost, high-yield micro LED production

Typical 200 mm GaN-on-Si epiwafer of ALLOS for micro LED



- **Excellent emission uniformity: < 0.6 nm sigma** ✓
- **High crystal quality: TDD ~2 x 10^8 cm^{-2}** ✓
- **Existing MQW from on-sapphire can be easily integrated** ✓
- **Flat wafers: < 30 µm bow for 725 µm thickness (200 mm)** ✓
- **No cracks, no residual strain** ✓
- **Large diameter: 200 mm and 300 mm** ✓

300 mm GaN-on-Si growth is NOT the future anymore!



ALLOS' technology is already scaled to 300 mm GaN-on-Si!

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Conclusion: GaN-on-Si is the material of choice for micro LED

Requirement for micro LED	GaN-on-sapphire	GaN-on-Si with ALLOS' quality
Micro LEDs are much smaller and thus more difficult to make Tiny size demands new processing skills	Conventional LED processing is insufficient ↓	Opens door for silicon industry process skills ✓
Micro LEDs require thin-film designs (substrate removal) Micro LEDs need substrate removal	Laser-lift-off and bonding cause yield issues ↓	High yield substrate removal and bonding ✓
Monolithically integrated displays need diameter to match CMOS Match CMOS wafer size	100 mm standard size and only max. 150 mm size ↓	Same size and bow like CMOS driver wafer ✓
'Square packing' becomes a crucial cost driver More transfer stamps & AR displays per wafer	Limited by available wafer size ↓	40 % cost saving / more displays with 300 mm ✓
Required yield levels make quantum leap of yield necessary Huge volume and zero failure need high yield	Conventional LED processing is insufficient ↓	Record uniformity and use of silicon industry yield ✓
Cost is hugely driven by yield in processing steps after epi Low cost is possible but only with high yield	Low cost but yield is low causing high cost ↓	Super uniform epiwafer increases yield downstream ✓

CSindustry awards

WINNER

2018 and 2019

Thank you very much for your attention!

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